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HY16F19 Series
User manual

High-Precision Mixed Signal Micro Controller
4x36 ~ 6x34 LCD Driver
32-bit Low Power Micro Controller
21-bit ENOB ΣΔADC
64Kb Flash ROM

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1. CHIP OVERVIEW

1.1. Brief introduction

The HY16F19 is a low-power and high-precision mixed signal micro controller (MCU) with LCD driver (Liquid Crystal Display), and is applicable to perform high-precision measurement and control; besides, the controller can work in a wide voltage range (2.2V-3.6V) and the clock of the controller can be up to 20MHZ; further, the controller has a built-in 64/32/16kbyte embedded Flash ROM and a 8/4/2kbyte SRAM. The HY16F19 series products integrate a high-precision 24-bit ΣΔ A/D converter, Rail-to-Rail OPAMP, 8-bit D/A converter, Hardware RTC and Multi-Comparator; moreover, the HY16F19 series products provide high-performance peripheral interfaces, such as the EAURT, SPI, I2C, GPIO and built-in power management system, etc, and support low-voltage detection and multiple peripheral interface wake-up functions. The HY16F19 series products are of low voltage, low power, low stand-by current, high integrity and high efficient operation, and support the 32-bit micro controller of the C/C++ development platform. Therefore, the HY16F19 series products can provide various resources for designers to design a low-current and low-cost mixed signal processing system.

The AFE circuit of the controller includes an 8-bit D/A converter, a Rail-to-Rail OPAMP and a Rail-to-Rail input comparator. In particular, 8-bit D/A converter has monotonicity, which is a step resistor, and the least significant bit (LSB) is close to 730 ohm and the resistor has the low-temperature coefficient. The Rail-to-Rail OPAMP has an input network, which is applicable for the differential analog circuit configuration, such as integrator, current-to-voltage converter, programmable gain amplifier and successive approximation A/D converter. The Rail-to-Rail input comparator can continuously monitor analog signals by extremely low power consumption; thus, it can serves as a power supply voltage monitor, external wake-up triggering source or capacitive touch key driver.

The 24 bits A/D converter with extremely low noise is embedded. Its maximal output rate is 10.24KSPS, its ENOB (Effective number of bit) is 21, and its minimal resolvable signal is 65nV RMS Noise (Root- Mean- Square). The programmable gain amplifier with low noise is used with the A/D converter together and the maximal gain is 128 times magnification. There is a built-in 4-bit A/D converter at the input of the A/D converter to expand the measurement range.

The power management provides selectable analogous regulating voltage, which can serve as reference voltage source or the power supply of a transducer. The working power source of the core of the CPU is also provided by the internal linear stabilized power supply. The charge pump is used to block the power interference from the system.

64Kbyte embedded Flash ROM can be used to execute programs or store data; the data can be still stored into the Flash ROM even if the Flash ROM is executing a program.

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A built-in 8kbyte SRAM is provided for the system to use.

The core of the 32-bit high-performance mixed signal micro controller can execute an instruction during each clock cycle, which can be up to 20MIPS (Millions of Instructions Per Second) and conform to low power consumption indicator. HYCON Technology provides convenient programming tools for users to write programs by C/C++ language or assembly language in the development platform. The chip has the circuit simulation function and provides a good environment for troubleshooting. The chip can work in 2.2V to 3.6V and -40℃ to 85℃.

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1.2. Type description table

The bit type description table of the register

Setting type	Description	Initial value
-	No Use	
RSV.	Reserve	
X	Unknown	
W	Write	
R	Read	
R0	Only Read 0	
R1	Only Read 1	
W0	Only Write 0	
W1	Only Write 0	
RW-0	Read/ Write	Initial 0
RW-1	Read/ Write	Initial 1
R0W-0	Read 0/ Write	Initial 0
R1W-1	Read 1/ Write	Initial 1
R-X	Read	Initial 1 or 0　Unknown

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2. FUNCTION OVERVIEW

2.1. Block diagram

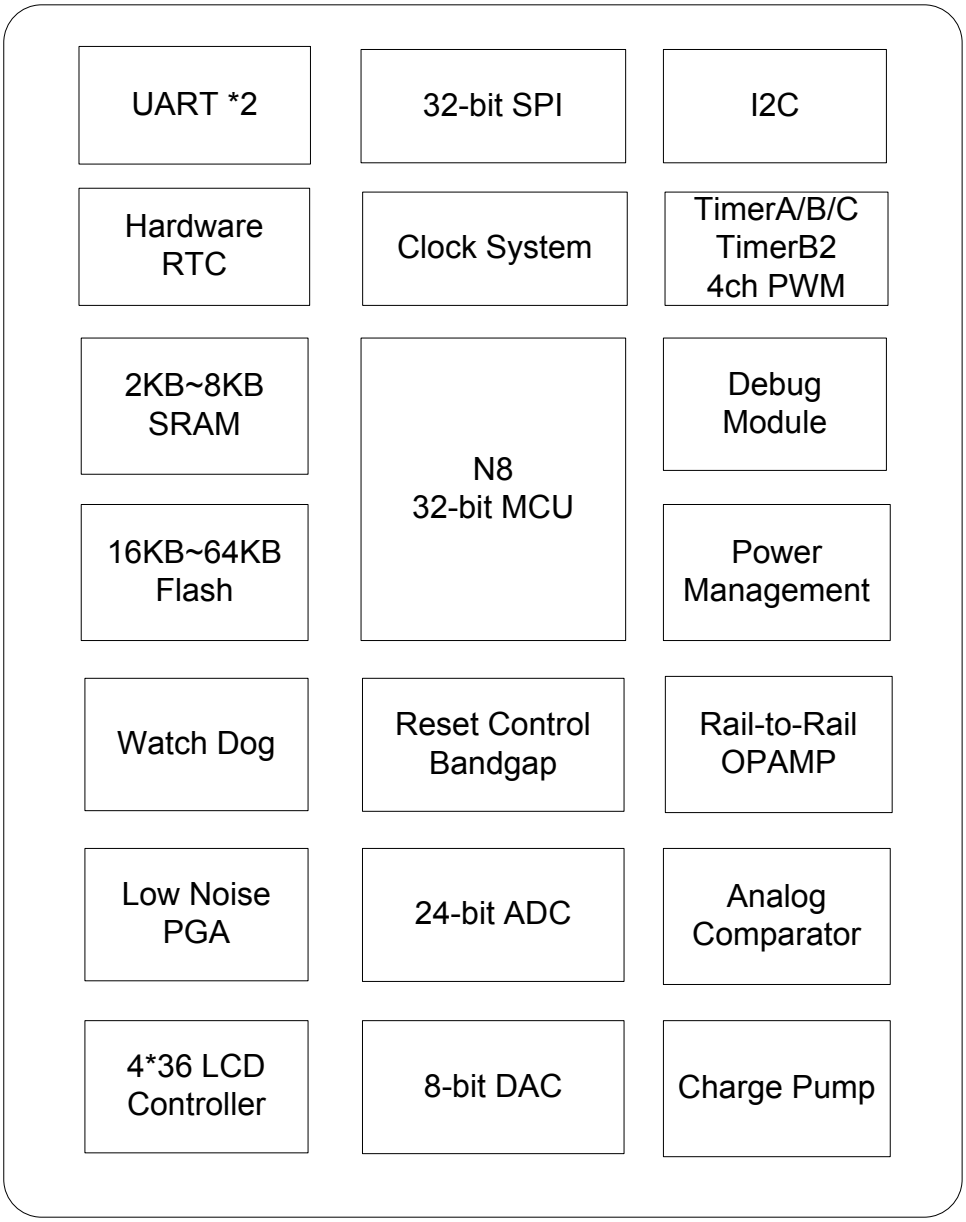

FIG. 2-1 Chip function structure diagram

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2.2. CPU core block diagram

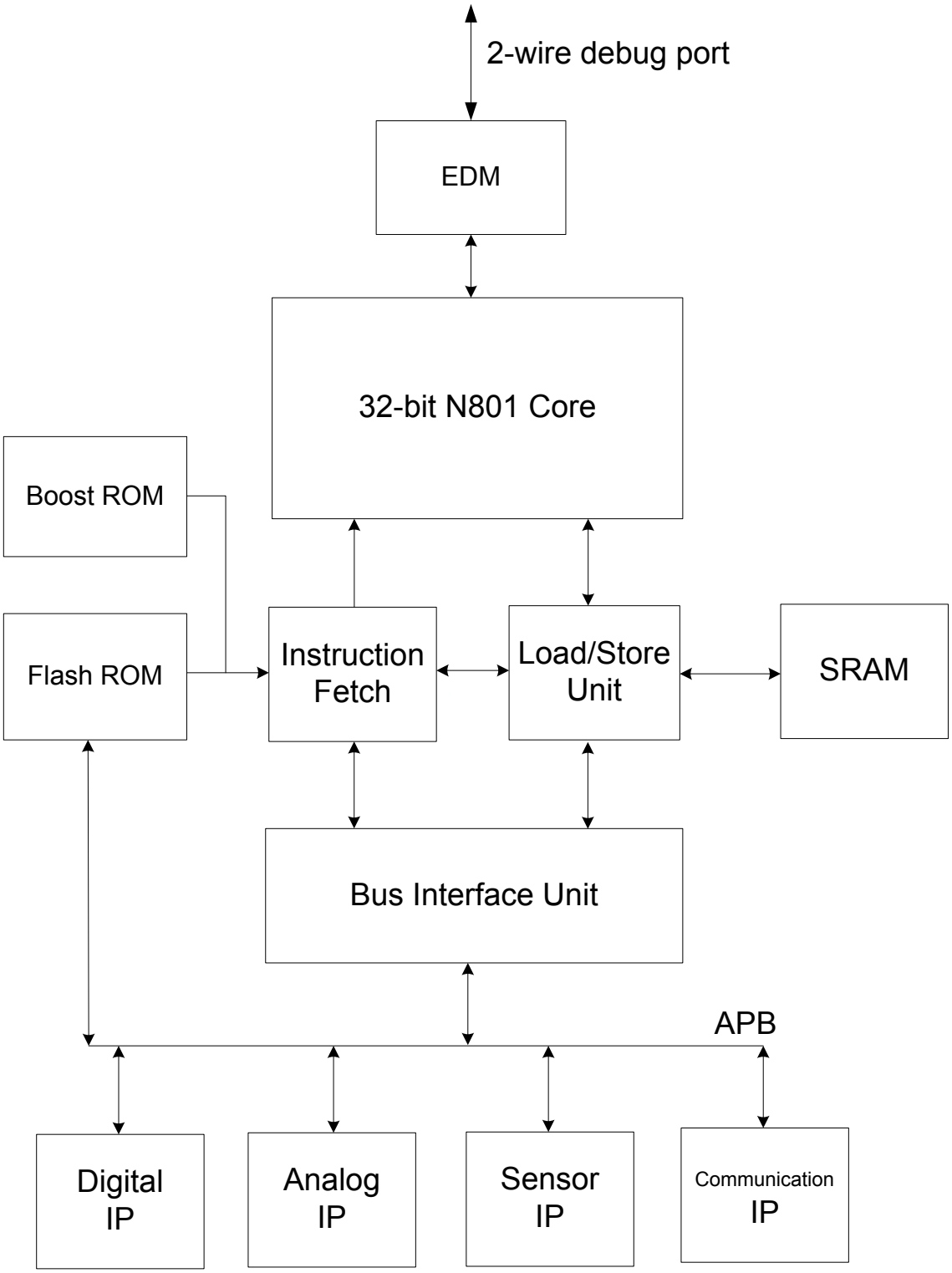

FIG. 2-2 CPU core block diagram

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3. MEMORY STRUCTURE

3.1. Memory description

The core of the CPU (Central Processing Unit) of HY16F19 series products is Andes N801 32-bit CPU. The allocation of the memory addresses of the micro controller is as follows:

0x00000 to 0x01FFF Static random-access memory (SRAM) (8K Byte)

0x40000 to 0x4FFFF SOC Register

0x80000 to 0x81FFF Boot ROM (8K Byte)

0x90000 to 0x9FFFF Main Program Flash ROM (64K Byte)

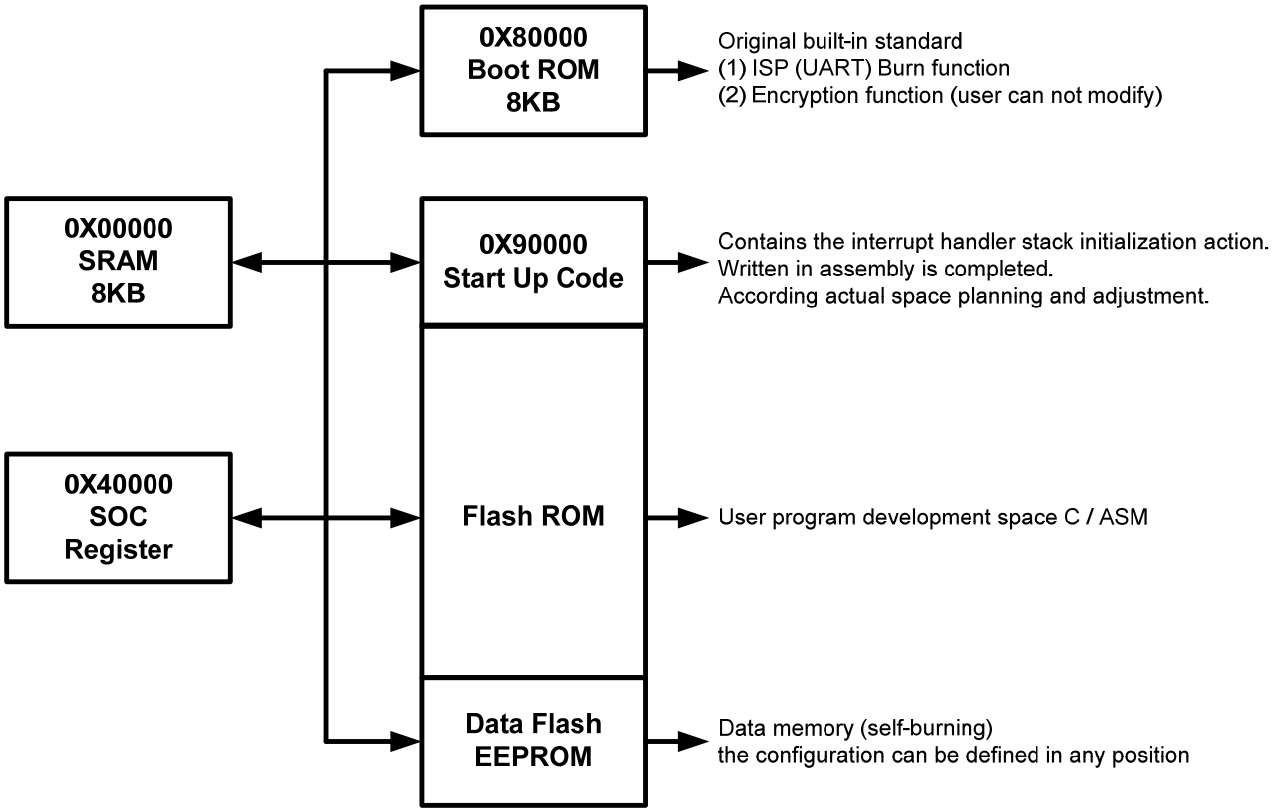

FIG. 3-1 Memory address allocation diagram

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3.2. Memory address

The detailed address allocation of the SOC registers of the micro controller is as follows:

Function module	Description	Base Address
INT	Interrupt Flag	0x40000
SoC	System control register	0x40100
CLK	Clock system control register	0x40300
PMU	Power management control register	0x40400
MC	Memory controller register	0x40600
PIO	GPIO port control register	0x40800
TMR	Timer register	0x40C00
UART	UART mode control register	0x40E00
SPI	SPI mode control register	0x40F00
I2C	I2C mode control register	0x41000
ADC	Analog-to-Digital module control register	0x41100
DAC	Digital-to-Analog module control register	0x41700
CMP	Comparator network module control register	0x41800
OPAMP	Operational amplifier control register	0x41900
RTC	Real time clock control register)	0x41A00

Table 3-1 SOC registers

Some important registers have MASK bits, as describe in FIG. 3.3. MASK is used to control written-in bits; only when the MASK bit corresponding to the control bit is <1>, the corresponding control bit can be written in, or the written-in operation will be invalid and cannot actually modify the value of the register, as shown in FIG. 3-2.

The total length of a register is 32-bit and most registers have 16 MASK bits. The MASK bits include two 8-bit groups, and each 8-bit group controls corresponding 8 control register bits. According to the content allocation of a register: BIT[31:24] controls BIT[23:16], and BIT[15:8] controls BIT[7:0]. Only when the MASK bit is <1>, the corresponding control bit can be validly written in.

For example, if a user wants to write 101010b in BIT[5:0] and the write value of the register should be: 0011111100101010b, where 00111111b are the MASK bits of BIT[5:0] and can make written-in corresponding control bits valid; and 00101010b are the values written in BIT[5:0].

INT Base Address + 0x10 (0x40010)									
Symbol	INTPT1 (PT1 Interrupt Control Register)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT17IE	PT16IE	PT15IE	PT14IE	PT13IE	PT12IE	PT11IE	PT10IE

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RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT17IF	PT16IF	PT15IF	PT14IF	PT13IF	PT12IF	PT11IF	PT10IF
RW	R0W-0	RW0-0							

FIG. 3-2 Basic structure of register

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3.3. Static random-access memory (SRAM)

HY16F198 has a 8Kbyte SRAM. The initial address is from 0x00000 to 0x02000. MCU can select to access one byte, half word or one word. MCU can access one word during each clock cycle.

3.4. Flash ROM

HY16F198 has a 64Kbyte embedded Flash ROM. The initial value is from 0x90000 to 0x9FFFF. User programmable codes are stored in the Flash ROM. A user needs to use CPU instructions to read and write the Flash ROM if wanting to edit the program codes of the Flash ROM. The user can store data at any positions between the blocks.

3.5. Bus interface unit

Regarding the structure of a bus, the reading and writing of the register are controlled by a 32-bit advanced peripheral bus (APB), which can write in 32-bit data during each clock cycle. In order to prevent from the existing data be covered when writing in new data, the user can use the MASK function to finish the operation.

As described in FIG. 3.3, the original data in BIT[7:0] of the register are 10101010b, and the written-in data are made valid via the MASK bits; when 0000111101010101b are written in BIT[15:0], the result will be 0000000010100101b, which means the MASK bit can only be set as 1b and the read value will be 0b; when 0101b are written in BIT[7:4], but the definition of BIT[15:13] is 000b; therefore, it means the write values of BIT[7:4] are invalid; when 0101b are written in BIT[3:0] and the definition of MASK BIT[11:8] is 1111b; therefore, it means the write values of BIT[3:0] can be valid.

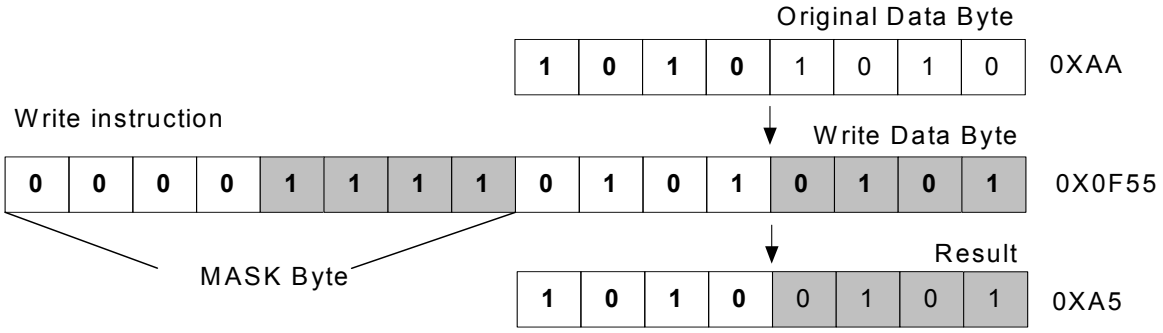
Original Data Byte
1 0 1 0 1 0 1 0
0XAA
Write instruction
Write Data Byte
0 0 0 0 1 1 1 1 0 1 0 1 0 1 0 1
0X0F55
Result
MASK Byte
1 0 1 0 0 1 0 1
0XA5

FIG. 3-3 Data flow structure

3.6. Boot ROM

8Kbyte Boot ROM is provided, and the initial value is from 0x80000 to 0x81FFF. The

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blocks are for boot codes, flash codes and security codes. When the chip is reset, the program timer will start from 0x80000. The software of the Boot ROM includes many information, such as system program protocol, security protocol and the like.

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3.7. Embedded debug module (EDM)

The embedded debug module (EDM) is a debug interface which can be used by the chip in the development environment. When the chip has no security protection, the user can transmit instructions to the MCU via EDM interface to read the information of the debug mode. EDM is the bridge of the communication between the chip and the computer The PC USB and the chip EDM are connected via HY-Protocol (USB control board) by only using a two-wire protocol interface. EDM can access the control register, general GPR register, SRAM DLM and Flash ROM ILM of a chip.

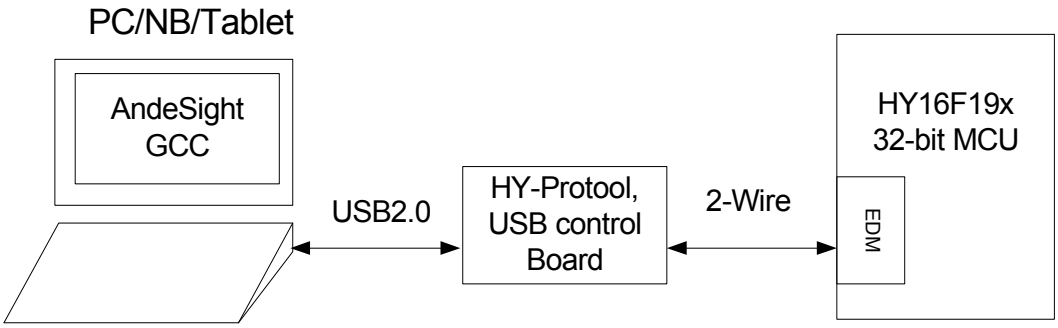

FIG. 3-4 Chip development connection diagram

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4. SOC REGISTER

4.1. Overall description

Manage the operating mode of the system and the reset status of the chip, such as WDT, external reset, under voltage reset, etc.

4.2. Register address

SoC Status Register Address	31	24	23	16	15	8	7	0
SoC Status Base Address + 0x04(0x40104)	-		-		MASK0		REG0	

-Reserved

4.3. Register function

Operate the register SoC[4] can set the operating mode of the system as SLEEP mode/IDEL mode/WAIT mode. The user can check the register SoC[3:0] to understand what the current operating mode of the system is. The setting of the operating mode of the chip will be specified at the chapter 25.

4.3.1. SOC register

SoC Status Base Address + 0x04 (0x40104)									
Symbol	SoC Status Register								
Bit	[31:24]					[23:16]			
Name	ICE Configuration					SoC Configuration			
RW	R-0Fh					R-C0h			
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	F_{PRG}	F_{CRst}	IDLE	$F_{SLP/IDLE}$	F_{WDog}	F_{RST}	F_{BOR}
RW	R0W-0	RW-0	RW0-0		RW-0	RW0-0			RW0-1

Bit	Name	Description	
Bit[06]	F_{PRG}	Power Good Flag	
		0	Normal
		1	Power Good has already been triggered before.
Bit[05]	F_{CRST}	CPU Core Reset Flag	
		0	Normal
		1	ICP Core has already been triggered before.
Bit[04]	IDLE	IDEL Mode Control Bit	
		0	Sleep Mode
		1	IDLE Mode
Bit[03]	$F_{SLP/IDLE}$	Sleep/Idle Flag (Low voltage reset or reset circuit reset can reset the bit.)	
		0	Normal

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		1	Sleep Mode or Idle Mode
Bit[02]	F_{WDT}	WDT Flag (Low voltage reset or external reset can clear the bit.)	
		0	Normal
		1	WDT is reset or interrupted.
Bit[01]	F_{RST}	External Reset Flag (Low voltage reset (BOR) can clear the bit.)	
		0	Normal
		1	PT4.0 reset or ICP software reset has occurred.
Bit[00]	F_{BOR}	Low Voltage Reset (BOR) Flag (The bit will be automatically cleared after the voltage of the chip is higher than 1.8V.)	
		0	Normal
		1	Low voltage reset has occurred.

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5. POWER MANAGEMENT

5.1. Overall description

Power management module includes a charge pump regulator, a wide BandGap reference, a narrow BandGap reference, a VDDA LDO, a VDD18 LDO and a reference output buffer. Chip VDD3V can work by only one voltage source between 2.2V and 3.6V. The power system can be classified into three parts: I/O circuit, analog circuit, and digital circuit. The power supply of the I/O circuit is driven by VDD3V. The power supply of the analog circuit is driven by the internal VDDA LDO. Finally, the power supply of the digital circuit is driven by VDD18 LDO.

When the MCU is under IDEL mode, it will use lowest power consumption to perform the memory operation of the register and the SRAM. During the IDEL mode, the wide BandGap reference, BOR and VDD18 LDO are enabled. If the MCU is under the automatic wake-up mode, the low-speed oscillator should be enabled.

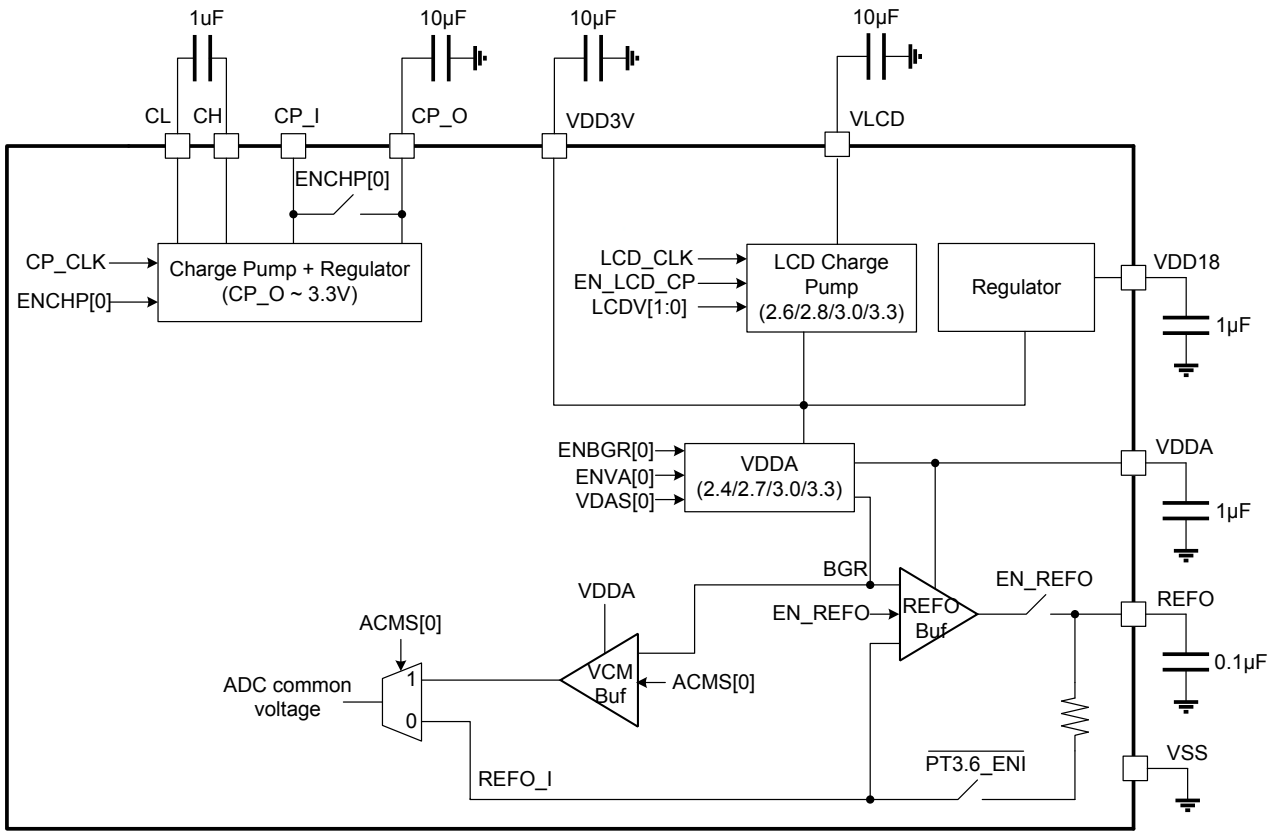

FIG. 5-1 Function block diagram

Chip operating voltages VDD3V and VDD18

The operating voltage of the chip is inputted via the pin VDD3V, and the voltage range is 2.2V~3.6V; besides, the pin should be connected to a 10uF ground capacitor, which can make VDD3V become more stable. If the operating voltage of the chip is used to drive a high current load, the operating voltage of the chip may be decreased and the chip may be reset; in this situation, it is necessary to enable the charge pump boost circuit to output a stable voltage to VDD3V via the CP_O pin so as to make sure the chip can work normally.

The VDD18 LDO output a stable voltage 1.8V via the VDD18 pin and the pin should be connected to a 1uF bypass capacitor. The VDD18 LDO has a low-power voltage mode; the register PMU[0] (VDDLP) should be set as 1 to achieve lowest power consumption. Before the control bit enters the IDEL mode, the user can set it as 1; after the MCU is wakened, the bit will be cleared to be 0.

VDDA voltage

The chip has a voltage regulator circuit LDO:VDDA, and the VDDA voltage should be enabled when using ADC. It can have different operating modes and different output voltages. It has four different operating modes; the first mode is to be short-circuited to the VDD3V; and the VDDA is close to the VDD3V during the mode. The second mode is Weak pull down; during the mode, the CDDA is close to the VSS. The third mode is High Z; and it is possible to input the voltage into the CDDA from outside but the inputted voltage should not exceed VDD3V. The four mode is adjustable voltage regulating mode LDO; during the mode, the VDDA can output four different voltages: 2.4V, 2.7V, 3.0V and 3.3V. For better performance, the voltage difference between VDD3V and VDDA. Should be higher than 0.2V and can drive at most 10mA. Additionally, it also needs to be connected to a 1uF bypass capacitor.

Low voltage detection circuit (BOR)

The BOR circuit is used to monitor the stability of the power system and the MCU. When the BOR detects the VDD3V and VDD18 are lower the detecting voltage of the BOR, the BOR will be triggered to reset the system and the chip; the chip will work normally until the BOR detects the operating voltage of the chip exceeds the voltage of the BOR.

Charge Pump

The charge pump regulator provides stable voltage for the chip, which can also be used to separate the power supply of the system from the power supply of the chip. Some applications will need to use high current external circuit, such as driving a DC motor; in this case, it is necessary to enable the charge pump to make sure the operating voltage of the chip is stable and the interference caused by the surge current from the inductors of the

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motor can be reduced.

So as to enable the charge pump, the register PMU[2] should be set as 1 and the ADC clock source should be enabled; the external circuit needs connect an external capacitor (Ccp2) in series between the CH/CL pins, and respectively connect an external ground capacitor to the CP_I/CP_O pins; the voltage regulating output end CP_O of the charge pump should be short-circuited to the operating voltage pin VDD3V of the chip. When the charge pump is working, the power supply is inputted from the CP_I to generate and output stable voltage from CP_O to the input of the VDD3V. If the charge pump is not enabled, the voltage of the CP_O will be equal to the voltage of the CP_I; and the voltage will be also outputted from the CP_O to the input of the VDD3V. If the charge pump boot circuit will not be used, it is not necessary to install the external capacitors Ccp2, Ccp1 and Ccp3; the operating voltage of the chip will be directly provided by VDD3V.

When the charge pump is working, it is suggested that the capacitances of the CH/CL pins are 1uF and cannot be lower than 0.1uF. It is suggested that the capacitance of the CP_O is at least ten times the capacitance of the capacitors connected in series between the CH/CL pins. If the capacitance of the CH/CL pins is 1uF, it is suggested that the capacitance of the CP_O is higher than or equal to 10uF. If the capacitance of the CP_O is large, the system will be more stable. The connection of the output of the CP_O and the pins of VDD3V should be done by short circuit from the external PCB.

BandGap reference voltage and common mode voltage (REFO)

When the VDDA is higher than 2.4V, the analog circuit can work. However, the analog circuit needs the current offset and the reference voltage. Therefore, the BandGap reference voltage should be enabled before the analog circuit is enabled; the BandGap reference voltage can be enabled by setting the register PMU[4](ENBGR) as 1. Only after the BandGap reference voltage is enabled, the common mode voltage (REFO) can effectively output 1.2V.

It is necessary to provide a common mode voltage (REFO) for the ADC to enable it. If the user wants to use the internal power supply, the ACMS should be set as 1; if the user wants to the external power supply, the ACMS should be set as 0 to output a common mode voltage (REFO). The user will need to use a reference voltage to drive the external circuit; therefore, the ENRFO should be set as 1 to output the common mode voltage to the pin; besides, the REFO is the BandGap reference voltage with buffer. The output voltage of the REFO pin is about 1.2V and has 200uA push-pull driving ability. It can drive a 22~1000nF big capacitor load. If the external REFO voltage output is used, the common mode voltage for the ADC can be provided by an external power supply; in this case, the ACMS can be set as 0 to save more power.

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The following table shows the voltage sources for all modules.

Table 5-1 Chip Power supply distribution

Block name	Voltage source	Block name	Voltage Source
32-bit CPU Core N801	VDD18	Timer A/B/C PWM	VDD18
08KB SRAM	VDD18	GPIO Port	VDD3V
64KB Flash ROM	VDD3V/ VDD18	24-bit SD ADC	VDDA
Clock System	VDD18	08-bit DAC	VDDA
Watch Dog Timer	VDD18	Rail-to-Rail OPAMP	VDDA
Hardware RTC	VDD18	Analog Comparator	VDD3V
Charge Pump	VIN		
BOR	VDD3V/ VDD18		
Band Gap/Reference	VDDA		
Hardware EUART	VDD18/VDD3V		
32-bit Hardware SPI	VDD18/VDD3V		
Hardware I2C	VDD18/VDD3V		

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5.2. Register address

Power Management Register Address	31	24	23	16	15	8	7	0
PMU Base Address + 0x00 (0x40400)	MASK1		REG1		MASK0		REG0	

5.3. Register function

5.3.1. Power management register (PMU)

Power Management Base Address + 0x00 (0x40400)									
Symbol	PMU (PMU Control Register)								
Bit	[31:28]	[27:24]	[20]		[19:18]		[17:16]		
Name	Rsv	Mask	Reg		VDAS		ENVA		
RW	R-0	R0W-0	RW-0		RW-0				
Bit	[15:08]		[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK		-	-	ENBGR	ACMS	ENCHP	ENRFO	VDDLP
RW	R0W-0		RW-0						

Bit	Name	Description	
Bit[19~18]	VDAS	VDDA output voltage selection	
		00	VDDA =2.4V
		01	VDDA =2.7V
		10	VDDA =3.0V
		11	VDDA =3.3V
Bit[17~16]	ENVA	VDDA LDO voltage source configuration for controlling the output voltage range of the VDDA.	
		00	High impedance (High Z)
		01	Internally short-circuited to the VDD3V; the output of the VDDA is close to the VDD3V
		10	Weak pull down; the output of he VDDA is close to the VSS.
		11	VDDA LDO; the output of the VDDA can be adjusted , which is decided by the VDAS.
Bit[04]	ENBGR	Band Gap voltage enablement control	
		0	Disable
		1	Enable (when ENVA=11b, it will be automatically enabled.)
Bit[03]	ACMS	ADC analog ground input source selection	
		0	External analog ground
		1	Internal analog ground (used with the ADC)
Bit[02]	ENCHP	Charge Pump enablement control	
		0	Disable
		1	Enable

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Bit[01]	ENRFO	Common mode voltage (REFO) enablement control	
		0	Disable
		1	Enable
Bit[00]	VDDLP	VDD18 LDO low-power control	
		0	Normal (the bit should be set as 0 after the SLEEP mode.)
		1	Low-power

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6. CLOCK SYSTEM

6.1. Overall description

The clock control system provides the clocks for the whole chip, including the system clocks (CPU clock, APB clock) and all peripheral operating clocks (timer, communication interface, RTC, analog circuit, etc.) Each function module has a clock switch controller, clock source selection and frequency divider. Under the SLEEP mode, the controller always closes the external crystal oscillators, internal crystal oscillators and system clocks to minimize the system power consumption.

The operating clock sources include the external crystal oscillators, internal HAO and LPO oscillators; with the frequency divider, the frequency sources of the CPU and the peripheral devices can be flexibly allocated and managed to adjust the power consumption of the chip in order to save the energy.

6.1.1. External oscillators

There are two external oscillators, including the high-speed crystal oscillator (HSXT) and the low-speed crystal oscillator (LSXT). The chip has two independent input pins for the external high-speed crystal oscillator and low-speed crystal oscillator; thus, the user can connect the two external oscillators to the chip at the same time. The external oscillator should be connected to a resistor in parallel, or the crystal oscillator will not work even if it is soldered at the pin; besides, the crystal oscillator can be connected to two 10~20pF ground capacitors and the capacitance of each capacitor is subject to the parasitic capacitor caused by the layout of the PCB.

The parallel resistor between the pins of the oscillator and the capacitor C2/C1 parameters of each pin of the oscillator will vary with the frequency, brand of the external crystal oscillator and the layout of the PCB. The following table lists suggested allocation of the R1/C1/C2 parameters and the frequency sources for your reference.

Type	Symbol	External crystal oscillator parameters				Instruction execution status	
		Frequency	R1/Ω	C1	C2	Sleep mode	Idle mode
Low-speed oscillator	LSXT	32768HZ	10M	10pF	10pF	Stop	Available
High-speed oscillator	HSXT	2~16MHZ	1M	10pF	10pF	Stop	Available

6-1 Suggest external crystal oscillator configuration

Matter needing attentions of using external crystal oscillators:

The operating voltage of the chip should be kept high when using a 16MHZ oscillator or above.

The stabilization time of the external 4MHZ/8MHZ crystal oscillators is about 25ms,

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and that of the external 32768HZ crystal oscillator is about 1.3s.

After the SLEEP instruction is executed, all external crystal oscillators will stop. Please pay attention to the I/O configuration of the pins when connecting to external crystal oscillators; when using the external crystal oscillators, the pins configuration should be set as input mode and no internal pull-up resistor is used so as to make sure they can work normally. Besides, the external resistors are necessary.

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6.1.2. Internal crystal oscillators HAO and LPO

The HAO is an external high-speed RC oscillator of the chip and its typical output frequency is 2MHZ/4MHZ/10MHZ/16MHZ; besides, it has several features, such as quick start, high anti-interference and low power consumption, etc. The output frequency of the HAO is adjustable; therefore, the user can adjust the output frequency of the HAO by software.

Matter needing attentions of using internal crystal oscillators:

The operating voltage of the chip should be kept high when using the 16MHZ HAO.
The output frequency of the HAO can be adjusted by modifying the register HAOTR.
The default oscillator of the chip is the internal 2MHZ HAO; the user can modify the default settings and change the output frequencies of other HAOs.
The stabilization time of the 4MHZ HAO is about 0.5ms;
After the SLEEP instruction is executed, all HAO oscillators will stop and enter the SLEEP mode.
After the IDEL instruction is executed, all HAO oscillators will not stop, but the CPU will enter the IDEL mode.
The LPO is the internal low-speed RC oscillator of the chip; its output frequency is 35kHZ and has low power consumption; it will immediately start after the chip is power-on or wakened; besides, it cannot be enabled; in other words, the LPO will keep working during the whole operation process of the chip.
The stabilization time of the LPO is about 510us and it is the only operating clock source of the WDT.
After the SLEEP instruction is executed, all LPO oscillators will stop.
After the IDEL instruction is executed, all LPO oscillators will not stop, but the CPU will enter the IDEL mode.
Typical output frequencies of the HAO and LPO are as shown in following Table 6-2.

Symbol	Frequency	Frequency source configuration			Instruction execution status	
		ENHAO[1]	HAO[1:0]	CKHS[1]	Sleep	Idle
HAO	2MHZ	1	00B	0	Stop	Workable
	4MHZ	1	01B	0	Stop	Workable
	10MHZ	1	10B	0	Stop	Workable
	16MHZ	1	11B	0	Stop	Workable
LPO	35KHZ	Start after the chip is power-on		CKLS=0	Stop	Oscillate

Table 6-2 Internal crystal oscillator configuration

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6.1.3. CPU and external peripheral operating frequency sources configuration

Both of the external and internal crystal oscillators can provide the frequency sources for the CPU and the frequency sources will be provided for the CPU after passing the frequency dividers. The chip can determine the frequency source of the CPU is the HS_CK or LS_CK via the frequency selector MCUCKS[1] and perform the frequency division via the frequency divider ENMCD[1]. Thus, there are multiple operating frequency modes for the CPU to select from to determine the instruction cycle of the chip.

Similarly, the external peripheral operating frequency sources are also provided by the external, internal crystal oscillators and the HS_CK or LS_CK passing the frequency dividers; or the frequency sources can be directly provided by the crystal oscillators, such as the WDT. As the external peripheral operating frequency configuration may vary with the different operations, please refer to the following figure for more information.

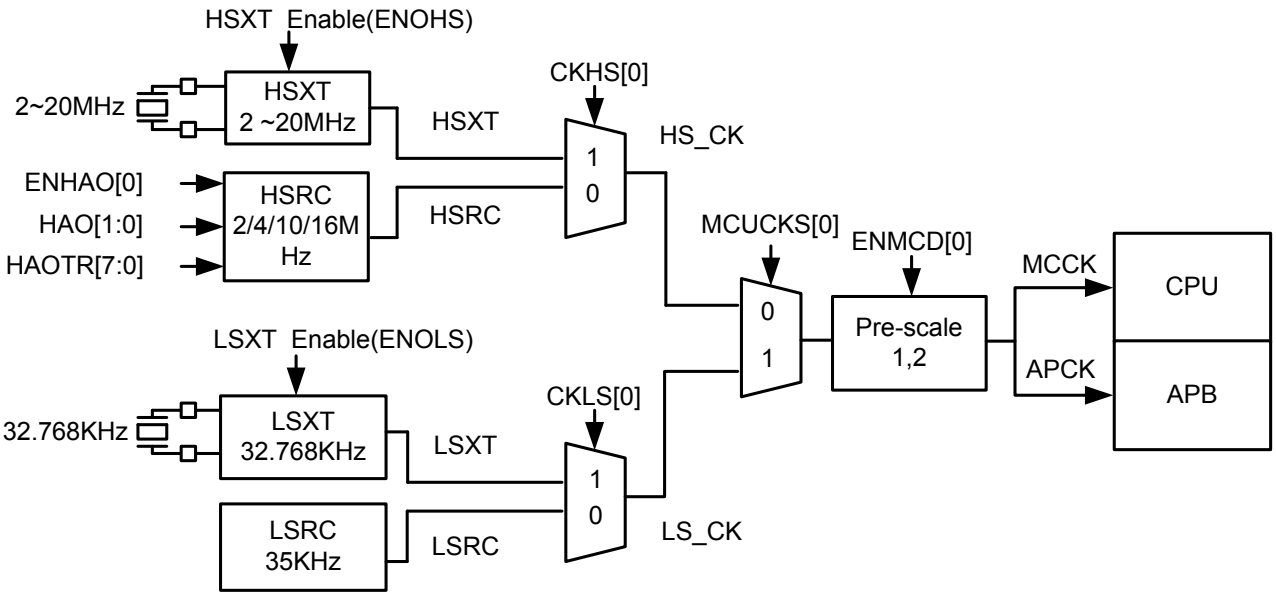

Table 6-1 CPU operating frequency source configuration diagram

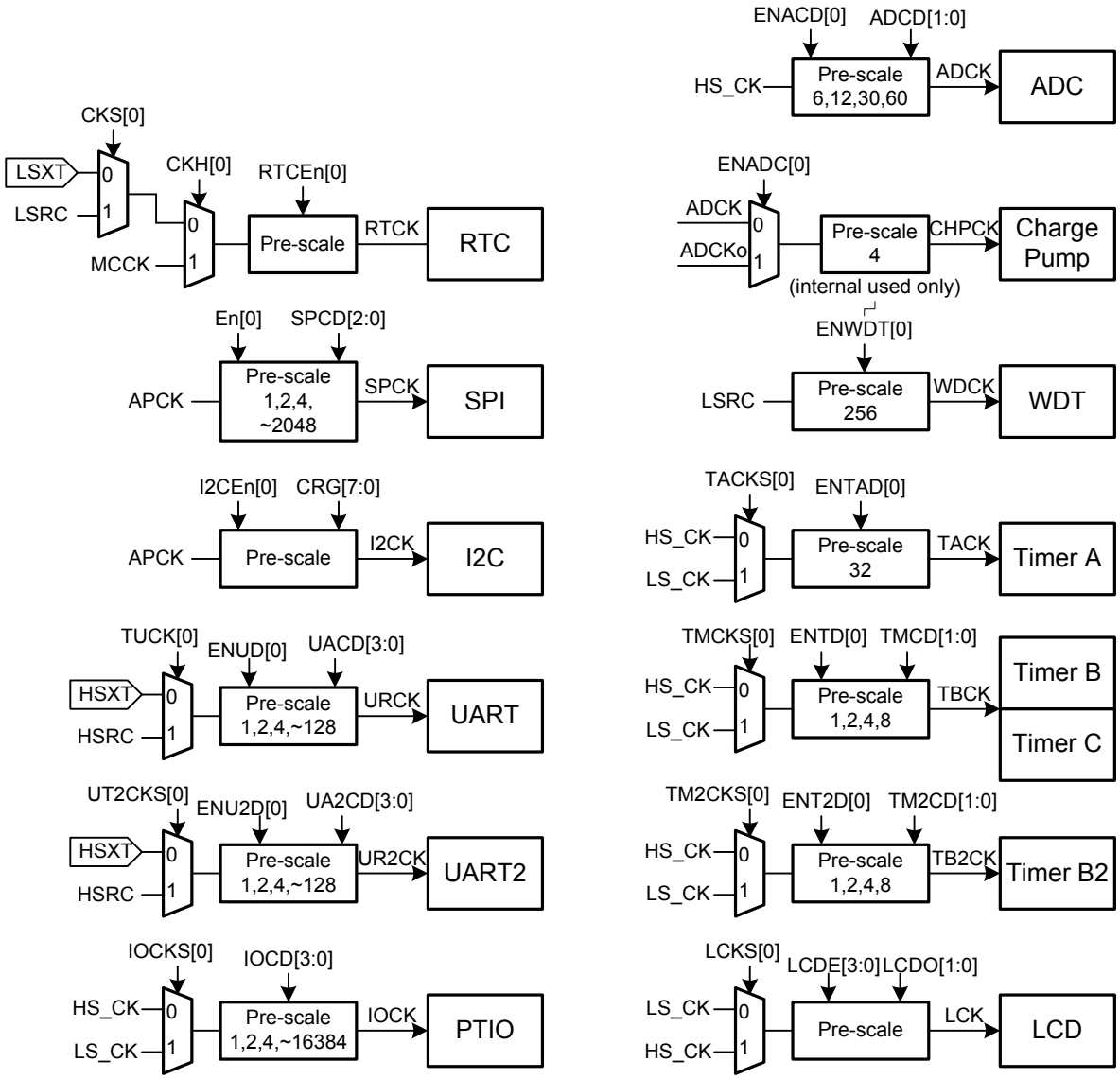

Table 6-2 External peripheral operating frequency configuration diagram

6.2. Register address

Clock Register Address	31 24	23 16	15 8	7 0
CLK Base Address + 0x00 (0x40300)	-	-	MASK0	REG0
CLK Base Address + 0x04 (0x40304)	-	-	-	HAOTR
CLK Base Address + 0x08 (0x40308)	MASK1	REG1	MASK2	REG2
CLK Base Address + 0x0C (0x4030C)	MASK3	REG3	MASK4	REG4
CLK Base Address + 0x10 (0x40310)	MASK5	REG5	MASK6	REG6
CLK Base Address + 0x14 (0x40314)	-	-	MASK7	REG7

-Reserved

6.3. Register function

6.3.1. Clock system register CLKCR0

Clock Base Address + 0x00 (0x40300)								
Symbol	CLK0 (Clock Control Register 0)							
Bit	[31:16]							
Name	RSV(Reserved)							
RW	R-0							
Bit	[15:8]	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Name	MASK	OHS_HS	CKLS	CKHS	HAO	ENOLS	ENOHS	ENHAO
RW	R0W-0	RW-0						RW-1

Bit	Name	Description	
Bit[7]	OHS_HS	External oscillator mode selection	
		0	HSXT<4MHz
		1	HSXT>4MHz
Bit[6]	CKLS	Chip low-speed frequency source selection	
		0	Internal low-speed oscillator (OSC_LSRC)
		1	External low-speed oscillator (OSC_LSXT)
Bit[5]	CKHS	Chip high-speed frequency source selection	
		0	External low-speed oscillator (OSC_HSRC)
		1	External high-speed oscillator (OSC_HSXT)
Bit[4~3]	HAO	Internal high-speed oscillator mode configuration	
		[00]	2MHz
		[01]	4MHz
		[10]	10MHz
		[11]	16MHz
Bit[02]	ENOLS	External low-speed oscillator enablement control	
		0	Disable
		1	Enable
Bit[01]	ENOHS	External high-speed oscillator enablement control	
		0	Disable
		1	Enable
Bit[00]	ENHAO	Internal high-speed oscillator enablement control	
		0	Disable
		1	Enable

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6.3.2. Clock system register CLKCR1

Clock Base Address + 0x04 (0x40304)		
Symbol	CLK1 (Clock Control Register 1)	
Bit	[31:16]	
Name	Reserved	
RW	R-0	
Bit	[15:8]	[7:0]
Name	Reserved	HAOTR
RW	R-0	RW-80H

Bit	Name	Description	
Bit[7:0]	HAOTR	Internal high-speed oscillator calibration control register	
		0	Set 0
		1	Set 1

1*LSB.Step = 0.125%

0000_0000 is the lowest speed.

1000_0000 is the default speed.

1111_1111 is the higher speed.

6.3.3. Clock system register CLKCR2

Clock Base Address + 0x08 (0x40308)								
Symbol	CLK2 (Clock Control Register 2)							
Bit	[31:24]	[23]	[22]	[21]	[20]		[19:16]	
Name	MASK	ENRTCK	-	TUCKS	ENUD		UACD	
RW	R0W-0	RW-0	-	RW-0				
Bit	[15:08]	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Name	MASK	TMCKS	ENTD	TMCD	TACKS	ENTAD	ENMCD	MCUCKS
RW	R0W-0	RW-0						

Bit	Name	Description	
Bit[23]	ENRTCK	RTC clock source control	
		0	Disable (The RTC register cannot be written in and unlocked.)
		1	Enable (The RTC register can be unlocked.)
Bit[21]	TUCKS	EUART clock source selection	
		0	HSXT: External high-speed oscillator
		1	HSRC: Internal high-speed oscillator
Bit[20]	ENUD	EUART clock source enablement control	
		0	Disable
		1	Enable

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Bit[19~16]	UACD	EUART clock source frequency divider configuration	
		0000	EUART clock source/ 1
		0001	EUART clock source/ 2
		0010	EUART clock source/ 4
		0011	EUART clock source/ 8
		0100	EUART clock source/ 16
		0101	EUART clock source/ 32
		0110	EUART clock source/ 64
		0111	EUART clock source/ 128
		1000 ~1111	Reserved
Bit[07]	TMCKS	Timer B,C clock source selection	
		0	HS_CK
		1	LS_CK
Bit[06]	ENTD	Timer B,C clock source enablement control	
		0	Disable
		1	Enable
Bit[5~4]	TMCD	Timer B,C clock source frequency divider configuration	
		00	clock/1
		01	clock/2
		10	clock/4
		11	clock/8
Bit[03]	TACKS	Timer A clock source selection	
		0	HS_CK
		1	LS_CK
Bit[02]	ENTAD	Timer A clock source frequency divider configuration	
		0	Disable the frequency divider
		1	Timer A clock/32
Bit[01]	ENMCD	MCU input clock source frequency divider configuration	
		0	MCU clock/1
		1	MCU clock/2
Bit[00]	MCUCKS	MCU input clock source selection	
		0	HS_CK
		1	LS_CK

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6.3.4. Clock system register CLKCR3

Clock Base Address + 0x0C (0x4030C)						
Symbol	CLK3 (Clock Control Register 3)					
Bit	[31:24]	[23:21]		[20]	[19:16]	
Name	MASK	-		IOCKS	IOCD	
RW	R0W-0	-		RW-0		
Bit	[15:08]	[7]	[6]	[5:4]	[3]	[2:0]
Name	MASK	ADCKP	ENACD	ADCD	ENSD	SPCD
RW	R0W-0	RW-0				

Bit	Name	Description	
Bit[20]	IOCKS	GPIO input clock source selection	
		0	HS_CK
		1	LS_CK
Bit[19~16]	IOCD	GPIO clock frequency divider configuration	
		0000	Disable
		0001	GPIO clock source/ 1
		0010	GPIO clock source/ 2
		0011	GPIO clock source/ 4
		0100	GPIO clock source/ 8
		0101	GPIO clock source/ 16
		0110	GPIO clock source/ 32
		0111	GPIO clock source/ 64
		1000	GPIO clock source/ 128
		1001	GPIO clock source/ 256
		1010	GPIO clock source/ 512
		1011	GPIO clock source/ 1024
		1100	GPIO clock source/ 2048
		1101	GPIO clock source/ 4096
		1110	GPIO clock source/ 8192
		1111	GPIO clock source/ 16384
Bit[7]	ADCKP	ADC clock phase shift(effective only at Core Clock/2 and Core Clock is HS_CK)	
		0	ADC Clock Rising Edge generates from Core Clock Low
		1	ADC Clock Rising Edge generates from Core Clock High
Bit[6]	ENACD	ADC clock switch	
		0	Disable
		1	Enable
Bit[5~4]	ADCD	ADC clock frequency divider configuration	

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		00	ADC clock source/ 6
		01	ADC clock source/ 12
		10	ADC clock source/ 30
		11	ADC clock source/ 60
Bit[3]	ENSD	SPI clock switch	
		0	Disable
		1	Enable
Bit[2~0]	SPCD	ADC clock frequency divider configuration	
		000	Reserved
		001	SPI clock source/ 2
		010	SPI clock source/ 4
		011	SPI clock source/ 8
		100	SPI clock source/ 32
		101	SPI clock source/ 128
		110	SPI clock source/ 512
		111	SPI clock source/ 2048

6.3.5. Clock system register CLKCR4

Clock Base Address + 0x10 (0x40310)						
Symbol	CLK4 (Clock Control Register 4)					
Bit	[31:24]	[23:22]	[21]	[20]	[19]	[18:16]
Name	MASK	LCDCPD	UT2CKS	ENU2D	-	UA2CD
RW	R0W-0	RW-0			-	RW-0
Bit	[15:08]	[7]	[6:4]		[3:1]	[0]
Name	MASK	-	LCDO		LCDE	LCKS
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[22~23]	LCDCPD	LCD charge pump regulator clock source selection	
		0	LS_CK / 1 or HS_CK/8 (LCKS determines LS_CK or HS_CK)
		1	LS_CK / 2 or HS_CK/16 (LCKS determines LS_CK or HS_CK)
		2	LS_CK / 4 or HS_CK/32 (LCKS determines LS_CK or HS_CK)
		3	LS_CK / 4 or HS_CK/32 (LCKS determines LS_CK or HS_CK)
Bit[21]	UT2CKS	UART2 clock source selection	
		0	HSXT: External high-speed oscillator
		1	HSRC: Internal high-speed oscillator
Bit[20]	ENUD2D	UART2 clock source enablement control	
		0	Disable

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		1	Enable
Bit[18~16]	UA2CD	UART2 clock source frequency divider configuration	
		0	UART2 clock source/ 1
		1	UART2 clock source/ 2
		2	UART2 clock source/ 4
		3	UART2 clock source/ 8
		4	UART2 clock source/ 16
		5	UART2 clock source/ 32
		6	UART2 clock source/ 64
		7	UART2 clock source/ 128
Bit[6~4]	LCDO	LCD clock source 1-stage frequency divider configuration	
		0	Disable
		1	LCD clock source/ 1
		2	LCD clock source/ 2
		3	LCD clock source/ 4
		4	LCD clock source/ 8
		5	LCD clock source/ 16
		6	LCD clock source/ 32
		7	Disable
Bit[3~1]	LCDE	LCD clock source 2-stage frequency divider configuration	
		0	LCD clock source/ 1
		1	LCD clock source/ 3
		2	LCD clock source/ 5
		3	LCD clock source/ 7
		4	LCD clock source/ 9
		5	LCD clock source/ 11
		6	LCD clock source/ 13
		7	LCD clock source/ 15
Bit[0]	LCKS	LCD clock source selection	
		0	LS_CK(always÷8)
		1	HS_CK(always÷64)

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6.3.6. Clock system register CLKCR5

Clock Base Address + 0x014 (0x403148					
Symbol	CLK5 (Clock Control Register 4)				
Bit	[31:16]				
Name	Reserved				
RW	R-0				
Bit	[15:8]	[7]	[6]	[5:4]	[3:0]
Name	Mark	TM2CKS	ENT2D	TM2CD	-
RW	R0W-0	RW-0			-

Bit	Name	Description	
Bit[7]	TM2CKS	Timer B2 clock source selection	
		0	HS_CK
		1	LS_CK
Bit[6]	ENT2D	Timer B2 clock source enablement control	
		0	Disable
		1	Enable
Bit[5~4]	TM2CD	Timer B2 clock source frequency divider configuration	
		0	Timer B2 clock source/ 1
		1	Timer B2 clock source/ 2
		2	Timer B2 clock source/ 4
		3	Timer B2 clock source/ 8

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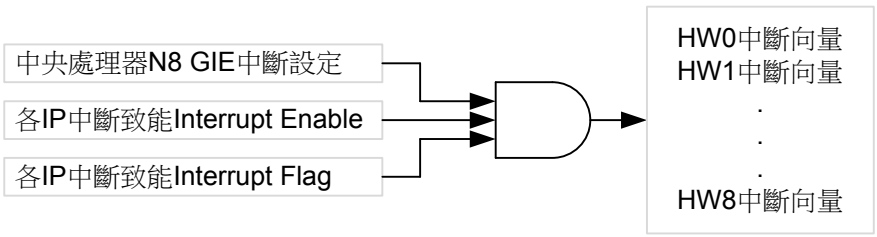
7. INTERRUPT CONTROL SYSTEM

7.1. Overall description

The interrupt module includes the interrupt startup controller, interrupt enable controller and interrupt event flag register to manage the overall interrupt service, such as communication interrupt, timer interrupt, ADC interrupt, comparator interrupt and IO external interrupt. The chip provides 9-stage interrupt source and also provides 9-stage interrupt vector priorities, including HW0, HW1…HW8 (from high priority to low priority). The interrupt service is composed of the interrupt event flag (INTF), interrupt event service intelligent startup (INTE), interrupt general control GIE and vector addresses HW0~HW8. When the interrupt event occurs and the interrupt event service is enabled, the program counter PC will turn to the interrupt service vector addresses HW0~HW8 of the program memory at the next instruction cycle to execute the interrupt service program.



CPU N8 GIE interrupt settings
Interrupt enable of each IP
Interrupt enable of each IP
Interrupt vector

FIG. 7-1 Interrupt service structure diagram

Detail operation description:

The user can set the corresponding interrupt enable bit to be 1 or clear the bit to enable or disable the corresponding interrupt function. The interrupt function can be enabled by setting the corresponding interrupt enable bit to be 1.

After the interrupt event takes place, the interrupt flag will be generated; the user can clear the flag to cancel the interrupt request.

It is necessary to set the global interrupt enable bit GIE=1, or any interrupt cannot be enabled.

The interrupt vector priority will be determined when multiple interrupt requests take place at the same time; the interrupt vector with high priority should be replied first.

During the execution of the interrupt vector service program, the high-level interrupt vector

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cannot terminate the current interrupt service to execute the high-level interrupt service; the high-level interrupt request can be executed only after the current interrupt vector service is finished.

After the interrupt service program is finished, it will automatically return to the program address where the interrupt occurred and continuously execute the program.

The corresponding interrupt vector program entry addresses of the interrupts of the chip are as shown in the following table.

Interrupt Vector Address	Vector	Interrupt Function
INT Base Address + 0x00 (I2C,UART,SPI communication interfaces)	HW0	void HW0_ISR(void)
INT Base Address + 0x04 (Timer ABC WDT HW RTC)	HW1	void HW1_ISR(void)
INT Base Address + 0x08 (ADC)	HW2	void HW2_ISR(void)
INT Base Address + 0x0C (CMP/OPA)	HW3	void HW3_ISR(void)
INT Base Address + 0x10 (PT1)	HW4	void HW4_ISR(void)
INT Base Address + 0x14 (PT2)	HW5	void HW5_ISR(void)
INT Base Address + 0x18 (Software Interrupt)	HW6	void HW6_ISR(void)
INT Base Address + 0x1C (UART2)	HW7	void HW7_ISR(void)
INT Base Address + 0x20 (TMB2)	HW8	void HW8_ISR(void)

7.2. Register address

Interrupt Register Address	31 24	23 16	15 8	7 0
INT Base Address + 0x00 (COM) (0x40000)	MASK0	REG0	MASK1	REG1
INT Base Address + 0x04 (TMR) (0x40004)	MASK2	REG2	MASK3	REG3
INT Base Address + 0x08 (ADC) (0x40008)	MASK4	REG4	MASK5	REG5
INT Base Address + 0x0C (CMP) (0x4000C)	MASK6	REG6	MASK7	REG7
INT Base Address + 0x10 (PT1) (0x40010)	MASK8	REG8	MASK9	REG9
INT Base Address + 0x14 (PT2) (0x40014)	MASK10	REG10	MASK11	REG11
INT Base Address + 0x18 (UART2) (0x40018)	MASK12	REG12	MASK13	REG13
INT Base Address + 0x1C (TMB2) (0x4001C)	MASK14	REG14	MASK15	REG15

-Reserved

7.3. Register function

7.3.1. Interrupt control register INTCOM

INT Base Address + 0x00 (0x40000)														
Symbol	INTCOM (Interrupt Control Register 0)													
Bit	[31:24]							[23:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK							-	I2CEIE	I2CIE	UTxIE	URxIE	STxIE	SRxIE
RW	R0W-0							-	RW-0					
Bit	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK							-	I2CEIF	I2CIF	UTxIF	URxIF	STxIF	SRxIF
	-	I2CEIR	I2CIR	UTxIR	TRxIR	STxIR	SRxIR							
RW	R-0							-	RW0-0					

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit1

5~8 are general registers.)

Bit	Name	Description	
Bit[21]	I2CEIE	I2C error interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	I2CIE	I2C interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	UTxIE	UART transmits (TX) interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	URxIE	UART receives (RX) interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	STxIE	SPI transmits (TX) interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	SRxIE	SPI receives (RX) interrupt enable control	
		0	Disable
		1	Enable
Bit[13]	I2CEIR	I2C interrupt error request	
		0	Normal
		1	Interrupt
Bit[12]	I2CIR	I2C interrupt request	
		0	Normal
		1	Interrupt
Bit[11]	UTxIR	UART Tx interrupt request	
		0	Normal
		1	Interrupt
Bit[10]	TRxIR	UART Rx interrupt request	
		0	Normal
		1	Interrupt
Bit[9]	STxIR	SPI Tx interrupt request	
		0	Normal
		1	Interrupt
Bit[8]	SRxIR	SPI Rx interrupt request	

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		0	Normal
		1	Interrupt
Bit[05]	I2CEIF	I2C error interrupt flag (level-trigger)	
		0	Normal
		1	I2C error takes place and interrupt occurs
Bit[04]	I2CIF	I2C interrupt flag (level-trigger)	
		0	Normal
		1	I2C interrupt occurs
Bit[03]	UTXIF	UART transmits (TX) interrupt flag (level-trigger)	
		0	Normal
		1	UART transmission (TX) interrupt occurs.
Bit[02]	URXIF	UART receives (RX) interrupt flag (level-trigger)	
		0	Normal
		1	UART receives (RX) interrupt occurs.
Bit[01]	STXIF	SPI transmission (TX) interrupt flag (level-trigger)	
		0	Normal
		1	SPI transmission (TX) interrupt occurs.
Bit[00]	SRXIF	SPI reception (RX) interrupt flag (level-trigger)	
		0	Normal
		1	SPI reception (RX) interrupt occurs.

7.3.2. Interrupt control register INTTMR

INT Base Address + 0x04 (0x40004)														
Symbol	INTTMR (Interrupt Control Register 1)													
Bit	[31:24]							[23:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK							-	RTCIE	WDTIE	TMC1IE	TMC0IE	TMBIE	TMAIE
RW	R0W-0							-	RW-0					
Bit	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK -	RTCIR	WDTIR	TMC1IR	TMC0IR	TMBIR	TMAIR	-	RTCIF	WDTIF	TMC1IF	TMC0IF	TMBIF	TMAIF
RW	R0W-0							-	RW0-0					

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit15~8 are general registers)

Bit	Name	Description	
Bit[21]	RTCIE	Real-time clock RTC interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	WDTIE	WDT interrupt enable control	
		0	Disable

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		1	Enable
Bit[19]	TMC1IE	TMC1 interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	TMC0IE	TMC0 interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	TMBIE	Timer TMB interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	TMAIE	Timer TMA interrupt enable control	
		0	Disable
		1	Enable
Bit[13]	RTCIR	RTC interrupt request	
		0	Disable
		1	Enable
Bit[12]	WDTIR	WDT interrupt request	
		0	Normal
		1	Enable
Bit[11]	TMC1IR	Timer C channel 1 interrupt request	
		0	Normal
		1	Enable
Bit[10]	TMC0IR	Timer C channel 0 interrupt request	
		0	Normal
		1	Enable
Bit[9]	TMBIR	TMB interrupt request	
		0	Normal
		1	Enable
Bit[8]	TMAIR	TMA interrupt request	
		0	Normal
		1	Enable
Bit[05]	RTCIF	Real-time clock RTC interrupt flag	
		0	Normal
		1	Real-time clock RTC interrupt occurs.
Bit[04]	WDTIF	WDT interrupt flag	
		0	Normal

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		1	WDT interrupt occurs.
Bit[03]	TMC1IF	TMC1 interrupt flag	
		0	Normal
		1	TMC1 interrupt occurs.
Bit[02]	TMC0IF	TMC0 interrupt flag	
		0	Normal
		1	TMC0 interrupt occurs
Bit[01]	TMBIF	Timer TMB interrupt flag	
		0	Normal
		1	Timer TMB interrupt occurs
Bit[00]	TMAIF	Timer TMA interrupt flag	
		0	Normal
		1	Timer TMA interrupt occurs.

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7.3.3. Interrupt control register INTADC

INT Base Address + 0x08 (0x40008)				
Symbol	INTADC (Interrupt Control Register 2)			
Bit	[31:24]		[23:17]	[16]
Name	MASK		-	ADCIE
RW	R0W-0		-	RW-0
Bit	[15:9]	[8]	[07:01]	[00]
Name	MASK		-	ADCIF
	-	ADCIR		
RW	R-0		-	RW0-0

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit 8 is general register.)

Bit	Name	Description	
Bit[16]	ADCIE	ADC converter interrupt enable control	
		0	Disable
		1	Enable
Bit[8]	ADCIR	ADC interrupt request	
		0	Normal
		1	Interrupt
Bit[00]	ADCIF	ADC converter interrupt flag	
		0	Normal
		1	ADC converter interrupt occurs.

7.3.4. Interrupt control register INTCMP

INT Base Address + 0x0C (0x4000C)						
Symbol	INTCMP (Interrupt Control Register 3)					
Bit	[31:24]			[23:18]	[17]	[16]
Name	MASK			-	CPOIE	OPOIE
RW	R0W-0			-	RW-0	
Bit	[15:10]	[9]	[8]	[07:02]	[01]	[00]
Name	MASK			-	CPOIF	OPOIF
	-	CPOIR	OPOIR			
RW	R-0			-	RW0-0	

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit9~8 are general registers.)

Bit	Name	Description	
Bit[17]	CPOIE	Multi-function comparator output (CPO) interrupt enable control	
		0	Disable
		1	Enable

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Bit[16]	OPOIE	Low-noise OP amplifier output (OPO) interrupt enable control	
		0	Disable
		1	Enable
Bit[9]	CPOIR	Multi-function comparator output (CPO) interrupt request	
		0	Normal
		1	Interrupt
Bit[8]	OPOIR	Low-noise OP amplifier output (OPO) interrupt request	
		0	Normal
		1	Interrupt
Bit[01]	CPOIF	Multi-function comparator output (CPO) interrupt flag	
		0	Normal
		1	Multi-function comparator output (CPO) interrupt occurs.
Bit[00]	OPOIF	Low-noise OP amplifier output (OPO) interrupt flag	
		0	Normal
		1	Low-noise OP amplifier output (OPO) interrupt occurs

7.3.5. Interrupt control register INTPT1

INT Base Address + 0x10 (0x40010)									
Symbol	INTPT1 (Interrupt Control Register 4)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT17IE	PT16IE	PT15IE	PT14IE	PT13IE	PT12IE	PT11IE	PT10IE
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK PT1 IR	PT17IF	PT16IF	PT15IF	PT14IF	PT13IF	PT12IF	PT11IF	PT10IF
RW	R-0	RW0-0							

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit15~8 are general registers.)

Bit	Name	Description	
Bit[23]	PT17IE	PT17IE: PT17 external interrupt enable control	
		0	Disable
		1	Enable
Bit[22]	PT16IE	PT16IE : PT16 external interrupt enable control	
		0	Disable
		1	Enable
Bit[21]	PT15IE	PT15IE : PT15 external interrupt enable control	
		0	Disable
		1	Enable

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Bit[20]	PT14IE	PT14IE : PT14 external interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	PT13IE	PT13IE : PT13 external interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	PT12IE	PT12IE : PT12 external interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	PT11IE	PT11IE : PT11 external interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	PT10IE	PT10IE : PT10 external interrupt enable control	
		0	Disable
		1	Enable
Bit[15:8]	PT1 IR	PT1 Bit7-0 interrupt request	
		0	Disable
		1	Enable
Bit[07]	PT17IF	PT17IF : PT17 external interrupt flag	
		0	Normal
		1	PT17 external interrupt occurs
Bit[06]	PT16IF	PT16IF : PT16 external interrupt flag	
		0	Normal
		1	PT16 external interrupt occurs
Bit[05]	PT15IF	PT15IF : PT15 external interrupt flag	
		0	Normal
		1	PT15 external interrupt occurs
Bit[04]	PT14IF	PT14IF : PT14 external interrupt flag	
		0	Normal
		1	PT14 external interrupt occurs
Bit[03]	PT13IF	PT13IF : PT13 external interrupt flag	
		0	Normal
		1	PT13 external interrupt occurs
Bit[02]	PT12IF	PT12IF : PT12 external interrupt flag	
		0	Normal
		1	PT12 external interrupt occurs
Bit[01]	PT11IF	PT11IF : PT11 external interrupt flag	

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		0	Normal
		1	PT11 external interrupt occurs
Bit[00]	PT10IF	PT10IF : PT10 external interrupt flag	
		0	Normal
		1	PT10 external interrupt occurs

7.3.6. Interrupt control register INTPT2

INT Base Address + 0x14 (0x40014)									
Symbol	INTPT2 (Interrupt Control Register 5)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT27IE	PT26IE	PT25IE	PT24IE	PT23IE	PT22IE	PT21IE	PT20IE
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK PT2 IR	PT27IF	PT26IF	PT25IF	PT24IF	PT23IF	PT22IF	PT21IF	PT20IF
RW	R0W-0	RW0-0							

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit15~8 are general registers.)

Bit	Name	Description	
Bit[23]	PT27IE	PT27IE : PT27 external interrupt enable control	
		0	Disable
		1	Enable
Bit[22]	PT26IE	PT26IE : PT26 external interrupt enable control	
		0	Disable
		1	Enable
Bit[21]	PT25IE	PT25IE : PT25 external interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	PT24IE	PT24IE : PT24 external interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	PT23IE	PT23IE : PT23 external interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	PT22IE	PT22IE : PT22 external interrupt enable control	
		0	Disable
		1	Enable

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Bit[17]	PT21IE	PT21IE : PT21 external interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	PT20IE	PT20IE : PT20 external interrupt enable control	
		0	Disable
		1	Enable
Bit[15:8]	PT2 IR	PT2 Bit 7-0 interrupt request	
		0	Disable
		1	Enable
Bit[07]	PT27IF	PT27IF : PT27 external interrupt flag	
		0	Normal
		1	PT27 external interrupt occurs
Bit[06]	PT26IF	PT26IF : PT26 external interrupt flag	
		0	Normal
		1	PT26 external interrupt occurs
Bit[05]	PT25IF	PT25IF : PT25 external interrupt flag	
		0	Normal
		1	PT25 external interrupt occurs
Bit[04]	PT24IF	PT24IF : PT24 external interrupt flag	
		0	Normal
		1	PT24 external interrupt occurs
Bit[03]	PT23IF	PT23IF : PT23 external interrupt flag	
		0	Normal
		1	PT23 external interrupt occurs
Bit[02]	PT22IF	PT22IF : PT22 external interrupt flag	
		0	Normal
		1	PT22 external interrupt occurs
Bit[01]	PT21IF	PT21IF : PT21 external interrupt flag	
		0	Normal
		1	PT21 external interrupt occurs
Bit[00]	PT20IF	PT20IF : PT20 external interrupt flag	
		0	Normal
		1	PT20 external interrupt occurs

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7.3.7. Interrupt control register INTUART2

INT Base Address + 0x18 (0x40018)								
Symbol	INTUART2 (Interrupt Control Register 6)							
Bit	[31:24]				[23:20]	[19]	[18]	[17:16]
Name	MASK				-	U2TxIE	U2RxIE	-
RW	R0W-0				-	RW-0		-
Bit	[15:12]	[11]	[10]	[9:8]	[7:4]	[3]	[2]	[1:0]
Name	MASK				-	U2TxIF	U2RxIF	-
	-	U2TxIR	U2RxIR	-				
RW	R-0				-	RW-0		

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit11~10 are general registers.)

Bit	Name	Description	
Bit[19]	U2TxIE	UART2 transmits (TX) interrupt enable control.	
		0	Disable
		1	Enable
Bit[18]	U2RxIE	UART2 receives (RX) interrupt enable control.	
		0	Disable
		1	Enable
Bit[11]	UTxIR	UART Tx interrupt request	
		0	Normal
		1	Interrupt
Bit[10]	TRxIR	UART Rx interrupt request	
		0	Normal
		1	Interrupt
Bit[03]	UTXIF	UART transmits (TX) interrupt flag (level-trigger).	
		0	Normal
		1	UART transmission (TX) interrupt occurs.
Bit[02]	URXIF	UART receives (RX) interrupt flag (level-trigger).	
		0	Normal
		1	UART reception (RX) interrupt occurs.

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7.3.8. Interrupt control register INTTMB2

INT Base Address + 0x1C (0x4001C)						
Symbol	INTTMB2 (Interrupt Control Register 7)					
Bit	[31:24]			[23:18]	[17]	[16]
Name	MASK			-	TMB2IE	-
RW	R0W-0			-	RW-0	-
Bit	[15:10]	[9]	[8]	[7:2]	[1]	[0]
Name	MASK -	TMB2IR	-	-	TMB2IF	-
RW	R-0			-	RW-0	

(When writing the register, the Bit15~8 are Mask; when reading the register, the Bit9 is general register.)

Bit	Name	Description	
Bit[17]	TMB2IE	Timer B2 interrupt enable control	
		0	Disable
		1	Enable
Bit[9]	TMB2IR	Timer B2 interrupt request	
		0	Normal
		1	Interrupt
Bit[1]	TMB2IF	Timer B2 interrupt flag (level-trigger)	
		0	Normal
		1	TMB2 transmission interrupt occurs.

7.4. Model program flow

(1)DrvTIMER_EnableInt(X) means enable the Timer system interrupt.

(2)DrvTIMER_ClearIntFlag(x) means clear the Timer system interrupt flag.

(3)Timer A/B/C and WDT belong to the HW1 interrupt , and the format is void HW1_ISR(void).

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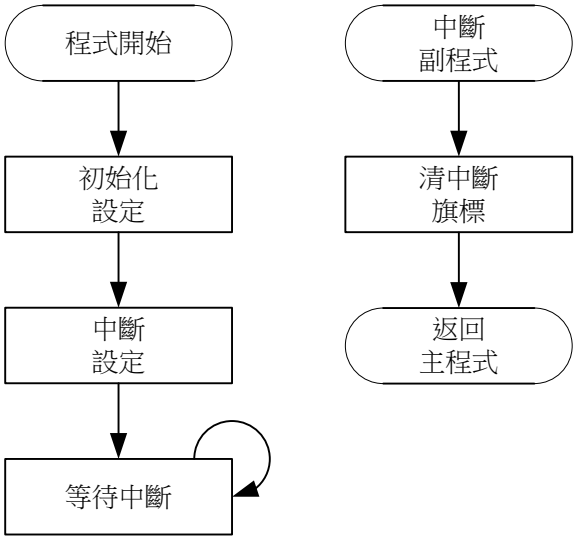

The program starts.
Initialization settings
Interrupt settings
Wait for interrupt
Interrupt the subprogram
Clear the interrupt flag
Return to the main program

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7.5. Model program function

Model name: the interrupt usage instruction and description

Model description: use the WDT interrupt service

7.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int i;
04
05  int main(void)
06  {
07      i=0x05;
08      DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);   //PT2_0~3 Set Output
09      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x05
10
11      DrvWDT_Open(E_IRQ,E_PRE_SCALER_D32);    //WDT IRQ open prescaler 32
12
13      DrvWDT_ClearWDT();                      //Clear WDT interrupt flag
14      DrvTIMER_EnableInt(E_WDT);              //WDT interrupt enable
15
16      SYS_EnableGIE(7);                       //Enable GIE
17
18      while(1);                               //Wait for Interrupt
20  }
21
22  void HW1_ISR(void)
23  {
24      DrvTIMER_ClearIntFlag(E_WDT);           //Clear WDT interrupt flag
25      i=i^0xF;                                //i XOR 0xF
26      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x0A~0x05
27  }
28
```

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8. WATCH DOG TIMER (WDT)

8.1. Overall description

The watch dog timer (WDT) is, as the name implies, the watcher of the chip, and its main function is to generate the wake-up event or execute basic reset function after the chip crashes accidentally.

Operation mode

The WDT overflows and then generate the reset signal to reset the chip.

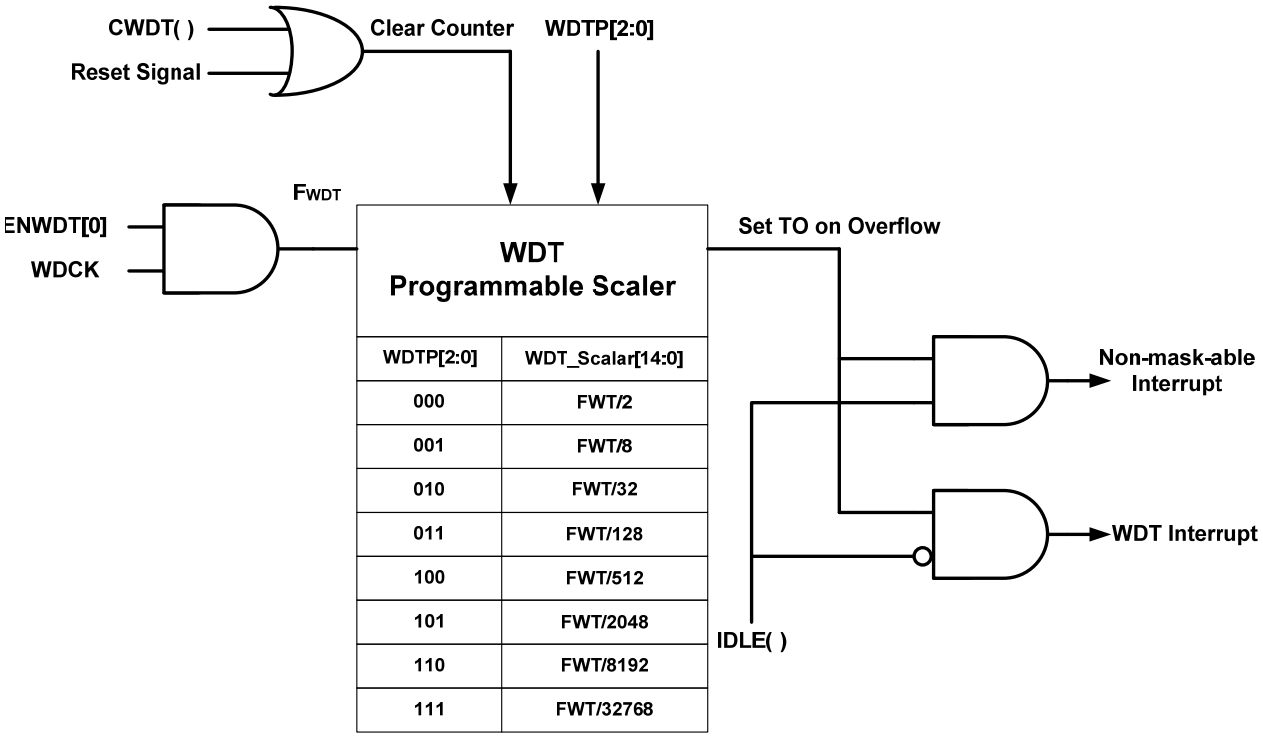
The WDT can be cleared by using software.

SLEEP mode

The WDT is disabled, and cannot work.

IDEL mode

The WDT overflows and then generate the interrupt event to wake up the chip.



WDTP[2:0]	WDT_Scalar[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

FIG. 8-1 WDT block diagram

8.1.1. WDT operating instruction

Setting the frequency divider WDTP[2:0] can determine the operating frequency and the overflow value of the WDT. After the WDT overflows, the WDT reset signal or interrupt event can be generated. The control bit WDTNMI[1] determines the reset signal or the interrupt request signal will be generated after the WDT overflows; if 0 is written in the bit, the WDT will generate the interrupt request signal. Please refer to the chapter about the interrupt control chapter for more information about the interrupt mode. The WDT can start up only when the chip is in operation; the WDT can start up by setting the control bit ENWDT[0] as <1>. It is necessary to enable the global interrupt control bit GIE before

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enabling the interrupt function.

The operating frequency source of the WDT is LPOCK; therefore, the calculation of the theoretical values of the operating frequency and the overflow value of the WDT is as follows:

WDT=LPOCK /256 /WDTP[2:0]　　（Equation 8-1）

LPOCK is the frequency of the internal low-speed RC oscillator; and WDTP is the frequency divider；

Assuming that LPOCK=33.9KHZ and WDTP=32768, the operating frequency of the WDT is:

33900Hz/256/WDT_PS(32768)=0.00404Hz

8.2. Register address

SoC Register Address	31	24	23	16	15	8	7	0
SoC Base Address + 0x08(0x40108)	WDTO1		WDTO0		MASK0		REG0	

8.3. Register function

8.3.1. WDT register WDTCR

SoC Base Address + 0x08 (0x40108)								
Symbol	WDTCR (WDT Control Register)							
Bit	[31]	[30:16]						
Name	-	WDTO						
RW	-	R-0						
Bit	[15]	[14:8]	[7]	[6]	[5]	[4]	[3]	[2:0]
Name	-	Mask	-	WDNMI	CLRWDT	ENWDT	-	WDTP
RW	-	R0W-0	-	RW1-0	RW-0	RW1-0	-	RW-7

Bit	Name	Description	
Bit[30~16]	WDTO	counter register of WDT	
		0	Set 0
		1	Set 1
Bit[06]	WDNMI	WDT interrupt operating mode selection	
		0	Timer mode
		1	Reset Mode; it cannot be switched to the Timer Mode again after switched to the Reset Mode.
Bit[05]	CLRWDT	WDT reset control	
		0	Disable
		1	Enable
Bit[04]	ENWDT	WDT enable control	

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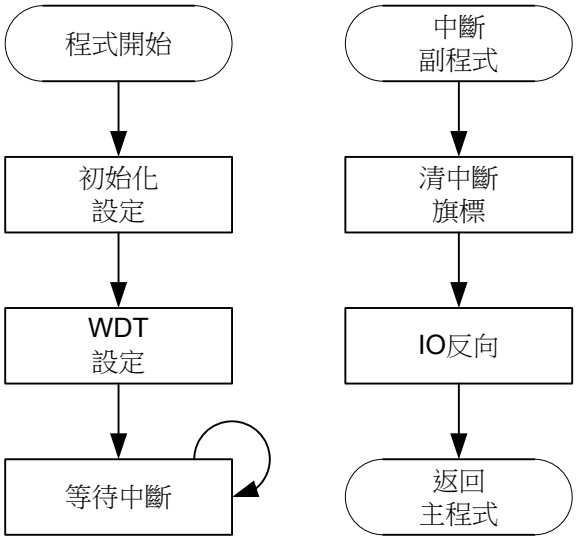
		0	Disable
		1	Enable(It cannot be disabled after enabled.)
Bit[2~0]	WDTP	WDT overflow value configuration	
		000	0 : WCLK / 2
		001	1 : WCLK / 8
		010	2 : WCLK / 32
		011	3 : WCLK / 128
		100	4 : WCLK / 512
		101	5 : WCLK / 2048
		110	6 : WCLK / 8192
		111	7 : WCLK / 32768

8.4. Model program flow

(1)Overclocking settings; only 35KHz is available (internal low-speed oscillator).
(2)DrvWDT_Open( ) will enable the WDT.
(3)DrvTIMER_EnableInt(E_WDT) means interrupting the enablement of the WDT.
(4)DrvTIMER_ClearIntFlag(E_WDT) means clearing the WDT interrupt flag.
(5)Timer A/B/C and WDT belong to the HW1 interrupt and the format is void HW1_ISR(void).



The program starts.
Initialization settings
WDT settings
Wait for interrupt
Interrupt the subprogram
Clear the interrupt flag

Reverse the I/O

Return to the main program

8.5. Model program function

Model name: the WDT usage instruction and description

Model description:

(1)Use the WDT interrupt.

(2)Each WDT interrupt will reverse the IO.

Ex: PT2=0x05 before the interrupt; PT2=0x0A after the interrupt.

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8.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int i;
04
05  int main(void)
06  {
07      i=0x05;
08      DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);   //PT2_0~3 Set Output
09      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x05
10
11      DrvWDT_Open(E_IRQ,E_PRE_SCALER_D32);    //WDT IRQ open prescaler 32
12
13      DrvWDT_ClearWDT();                      //Clear WDT interrupt flag
14      DrvTIMER_EnableInt(E_WDT);              //WDT interrupt enable
15
16      SYS_EnableGIE(7);                       //Enable GIE
17
18      while(1);                               //Wait for Interrupt
20  }
21
22  void HW1_ISR(void)
23  {
24      DrvTIMER_ClearIntFlag(E_WDT);           //Clear WDT interrupt flag
25      i=i^0xF;                                //i XOR 0xF
26      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x0A~0x05
27  }
28
```

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9. TIMER A

9.1. Overall description

Timer A is a 16-bit up counter and can be operated in operation mode and IDEL mode. It can be used to generate different output frequencies.

Main features:

Up counter

16-stage overflow values are available to be selected.

Overflow generates an interrupt event.

The values of the counter can be read.

Initial configuration of Timer A(TMA):

TMA is a 16-bit up counter. Its input clock source is the TACK and it will perform the counting according to each rising edge of the TACK and the frequency of the input clock source is controlled by the clock system management module. The function of the TMA can be enabled or disabled by setting the control bit ENTA[1] as 1 or 0.

The overflow value of the TMA can be adjusted by the frequency divider TAS[3:0]; the user can change the overflow value by modifying the value of the frequency divider TAS to generate the counting values with different frequencies. The control bit TACLR[1] is set as 1 but the TMA is reset and the counter register becomes 0; after the counter register is cleared, the control bit TACLR will automatically become 0.

After the TMA overflows, the interrupt request will be generated and the TMA interrupt flag will be set as <1>; if the TMA interrupt function is enabled and the global interrupt control bit is set as `, the chip will enter the TMA interrupt service event in response to the TMA interrupt request. The TMA interrupt request can be cancelled by clearing the TMA interrupt flag; in this way, the chip will not reply the TMA interrupt. Under the IDEL mode, the TMA interrupt can be used to wake up the chip. Under the SLEEP mode, the TMA interrupt is not available.

The TMA has a 16-stage frequency dividing configuration, which allows the TMA to have a wide counting range; the calculation of the overflow value of the TMA is as follows:

TAR[15:0]=1/（TACK/32/TAS[3:0]） （Equation 9-1）

The TACK is the input clock source of the TMA and the TAS[3:0] is the frequency dividing value;

Assuming the TMA selects the LS_CK, and the LS_CK is from the LPO; then TACK=35KHZ, TAS[3:0]=1001B=/1024 and the theoretical value of the overflow value of the Timer A:

35000Hz/32/TAS(1024)=35000Hz/32/1024=1.068Hz

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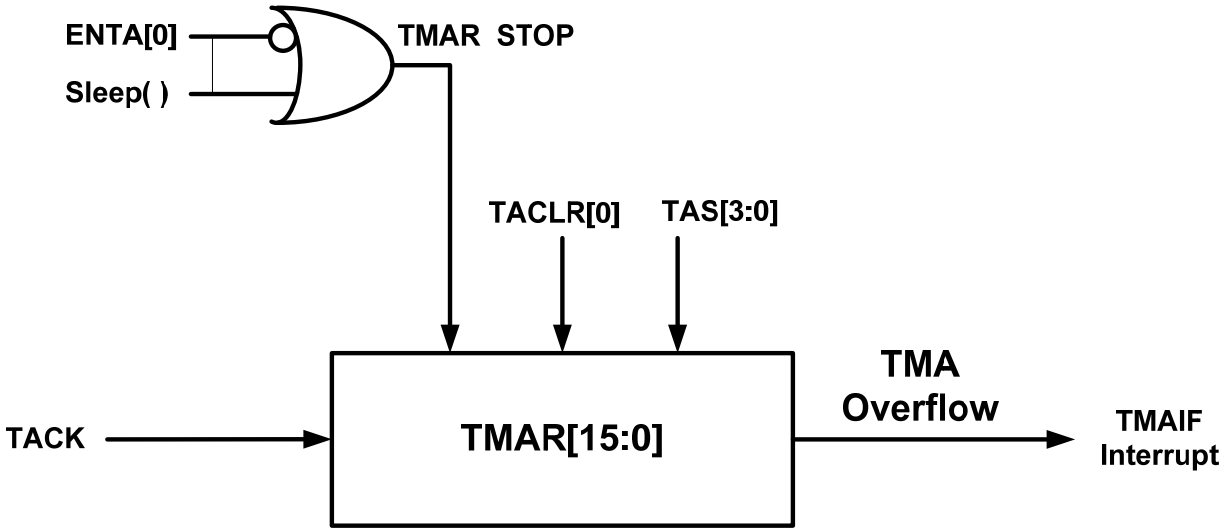

TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

FIG. 9-1 Timer A block diagram

9.2. Register address

TMA Register Address	31	24	23	16	15	8	7	0
TMA Base Address + 0x00(0x40C00)	TAR1		TAR0		MASK0		REG0	

9.3. Register function

9.3.1. Timer A register TMACR

TMA Base Address + 0x00 (0x40C00)						
Symbol	TMACR(TMA Control Register)					
Bit	[31:16]					
Name	TAR					
RW	R-0					
Bit	[15:8]	[7]	[6]	[5]	[4]	[3:0]
Name	MASK	-	Reg	ENTA	TACLR	TAS
RW	R0W-0	-	RW-0			RW-Fh

Bit	Name	Description
Bit[31-16]	TAR	Timer A Counter counting value

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		TAR[31:16] are the counting values of the 16-bit Timer A, and the output value can be MSB to LSB.	
Bit[5]	ENTA	Enable the Timer A	
		0	Disable
		1	Enable
Bit[4]	TACLR	Clear the counting value of the Timer A	
		0	Normal
		1	Clear (After the bit is cleared, the bit will automatically become 0).
Bit[3~0]	TAS	Timer A frequency divider configuration	
		0000	Timer A clock/2
		0001	Timer A clock/4
		0010	Timer A clock/8
		0011	Timer A clock/16
		0100	Timer A clock/32
		0101	Timer A clock/64
		0110	Timer A clock/128
		0111	Timer A clock/256
		1000	Timer A clock/512
		1001	Timer A clock/1024
		1010	Timer A clock/2048
		1011	Timer A clock/4096
		1100	Timer A clock/8192
		1101	Timer A clock/16384
		1110	Timer A clock/32768
		1111	Timer A clock/65536

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9.4. Model program flow

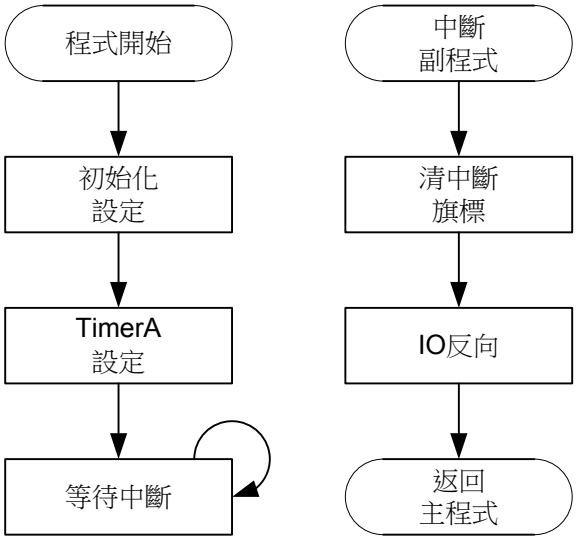
The default value of the overclocking setting is 2MHz (internal high-speed oscillator), and can be up to 20MHz@2.6V.

The HYCON C Library is adopted and the DrvTMA_Open(X,Y) can enable the TimerA IP and the Timer A Clock, where X stands for the TMAR frequency dividing and if 15 is selected, it will be divided by 65536; Y is to select the high-speed or low-speed to enter the Timer A.

HYCON C Library DrvTIMER_EnableInt(E_TMA) means enabling the Timer A interrupt.

HYCON C Library DrvTIMER_ClearIntFlag(E_TMA) means clearing Timer A interrupt flag.

Timer A/B/C and WDT belong to the HW1 interrupt and the format is void HW1_ISR(void).



The program starts.

Initialization settings

TimerA settings

Wait for interrupt

Interrupt the subprogram

Clear the interrupt flag

Reverse the I/O

Return to the main program

9.5. Model program function

Model name: Timer A usage instruction and description

Model description:

Use Timer A interrupt.

Each Timer A interrupt will reverse the IO.

Ex: PT2=0x05 before the interrupt and PT2=0x0A after the interrupt.

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9.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int i;
04
05  int main(void)
06  {
07      i=0x05;
08      DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);   //PT2_0~3 Set Output
09      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x05
10
11      DrvTMA_Open(15,0);                      //Timer A Overflow
12                                              //15 : taclk/65536/32;TMRDV=÷32
13                                              // 0 : HS_CK
14
15      DrvTIMER_ClearIntFlag(E_TMA);           //Clear Timer A interrupt flag
16      DrvTIMER_EnableInt(E_TMA);              //Timer A interrupt enable
17
18      SYS_EnableGIE(7);                       //Enable GIE
20
21      while(1);                               //Wait for Interrupt
22  }
23
24  void HW1_ISR(void)
25  {
26      DrvTIMER_ClearIntFlag(E_TMA);           //Clear TMA interrupt flag
27      i=i^0xF;                                //i XOR 0xF
28      DrvGPIO_SetPortBits(E_PT2,i);           //PT2 Output i=0x0A~0x05
29  }
30
```

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10. TIMER B

10.1. Overall description

The Timer B is a 16-bit counter, which can be used to perform time counting, time controlling, clock generating and time delaying, etc. It will generate the interrupt signal when the counting flow takes place, and the program can read the current counting value of the TMB; besides, the TMB can be also used to generate the waveform of the PWM. It can be operated under the operation mode and the IDEL mode.

The 16-bit counter register of the Timer B can be separated into two independent 8-bit counter registers; thus, the TMB has four counting methods:

16-bit up counting method, which can generate the interrupt signal;

16-bit counting method; it will increase to the overflow value and then decrease to 0, which can generate the interrupt signal;

Two independent 8-bit up counting methods; the low 8-bit counter overflows and then the high 8-bit counter is automatically added by 1, which can generate the interrupt signal;

Moreover, the TMB has three counter overflow controller: TBC0, TBC1 and TBC2. TMB can also serve as the PWM waveform generator, which can provide two PWM waveforms PWM0/PWM1; and each has multiple operation modes and can satisfy different PWM output requirements; the operation modes are as follows:

PWMA /PWMB /PWMC /PWMD /PWME /PWMF /PWMG

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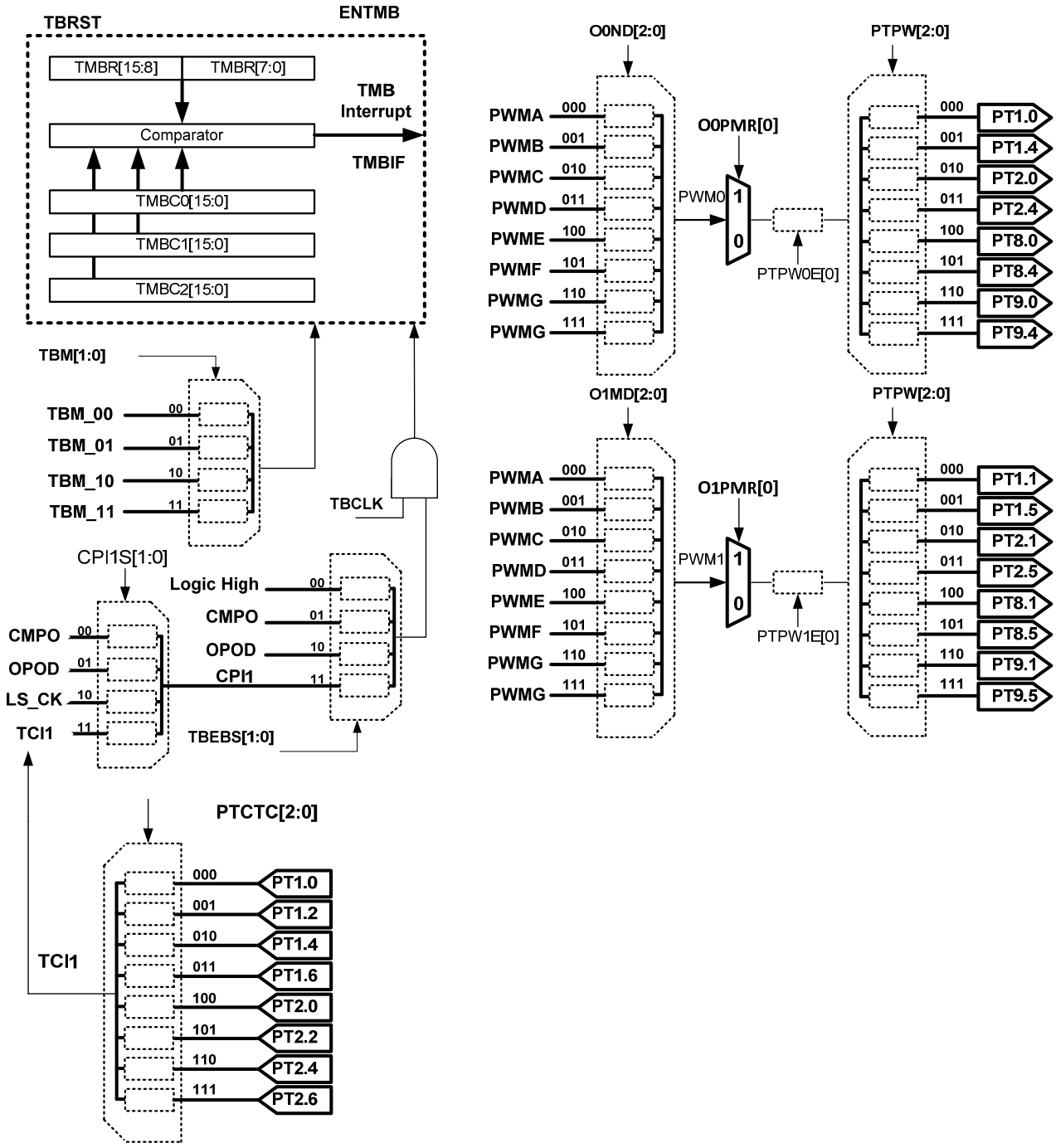

FIG. 10-1 Timer B block diagram

10.1.1. Timer mode

The Timer B is a 16-bit up counter, which can be used to generate the PWM waveforms. It can be used to perform the time counting, time controlling, clock generating, etc., and can generate the interrupt signal when the counter overflow takes place. The TMB can be operated under the operation mode and the IDEL mode.

It has four different counting methods, and can generate the counting values with different frequencies:

16-bit up counting method, which can generate the interrupt signal;

16-bit counting method; it will increase to the overflow value and then decrease to 0, which can generate the interrupt signal;

Two independent 8-bit up counting methods; the low 8-bit counter overflows and then the high 8-bit counter is automatically added by 1, which can generate the interrupt signal;

It has four different counting-trigger signal sources, which can be applied to count different events:

Continuous counting method is always enabled;

The comparator outputs (CMPO) high-potential trigger.

The OP amplifier outputs (OPOD) high-potential trigger.

The Timer C outputs (CPI1) high-potential trigger.

The operating clock source of the TMB is HS_CK or LS_CK, which will pass through the frequency divider to generate the frequency source TBCLK to provide the operating frequency for the TMB. It provides the setting frequency divider TMCD[1:0], which can set different counting cycles for the TMB. The clock source of the TMB can be set at the clock system control module.

TBR：16-bit timer/counter register

The TBR is a 16-bit timer/counter register, which can be separated into two independent 8-bit timer/counter registers in order to satisfy the four different counting methods of the TMB. The TBR will crease or decrease at each rising edge of the TBCLK; under different counting methods, the TBR will increase or decrease according to different conditions. TBR can be automatically cleared by setting the control bit TBRST[1] as <1> and the control bit TBRST will automatically become 0 after the TBR is cleared. The program can also read the current counting value of the TBR for other purposes.

The TBEN is the enable control signal of the TMB. If the bit is set as 1, the counting function of the TMB will be enabled; if the bit is set as 0, the counting function of the TMB will be disabled.

The TBEBS[1:0] is the counting-trigger signal source controller; the controller can provide four different counting-trigger signal sources.

TBM[1:0] is the counting method controller of the TMB; the controller can provide four

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different counting methods. The TBRST is the control bit of the TMB counter register. If the bit is set as <1>, the counter register will be automatically cleared and then the bit will automatically become 0.

Operating configuration when TMB serves as a timer/counter:

Set the operating clock source of the TMB and set the control bits 0x40308[6](ENTD) and 0x40308[5:4](TMCD);

Select the counting mode and set the control bit TBM[1:0];

Select the counting-trigger signal source and set the TBEBS[1:0]; as a timer, it can be set as 00b, which means it is always enabled and continuously perform counting;

Set the timer/counter overflow value is TBC0[15:0];

Set the control bit TBRST as <1> to clear the counting register;

Enable the TMB and the control bit TBEN is set as <1>.

The calculation of the theoretical overflow value of the Timer B:

T = TBC0*1 / TBCLK; TBCLK=HS_CK(or LS_CK) / TMCD; (Equation 10-1)

then

T=TBC0*TMCD / HS_CK(or LS_CK); (Equation 10-2)

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The TMB has four different counting methods, and different counting method have different overflow conditions, which will be specified later.

TMB counting method 0

When TBM [1:0] =00, the TBR serves as a 16-bit up counter. Under the mode, the TBR will be automatically added by 1 at each rising edge of the TBCLK; if the counting value of the TBR is higher than TBC0, the TBR will become 0 at the next rising edge and the timer interrupt flag TMBIF is set as <1>; if the interrupt function of the TMB and the global interrupt function are enabled, the chip will reply the TMB interrupt. Then, the TMB will restart the up counting. The schematic view of the counting waveform of the mode is as shown in the follow figure.

The counting cycle calculation method of the TMB under the mode: T=TBC0*TMCD / HS_CK(or LS_CK)

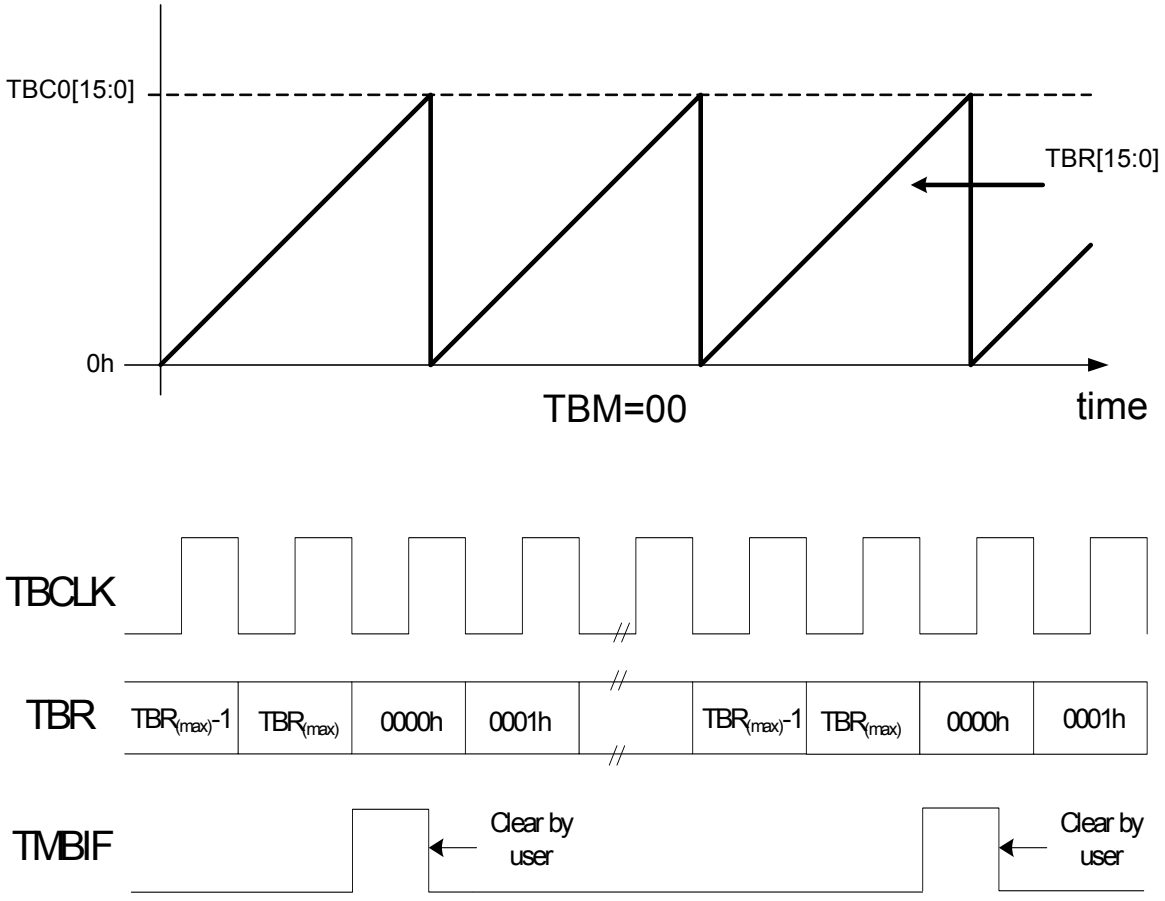

FIG. 10-2 Schematic view of counting waveform of counting method 0

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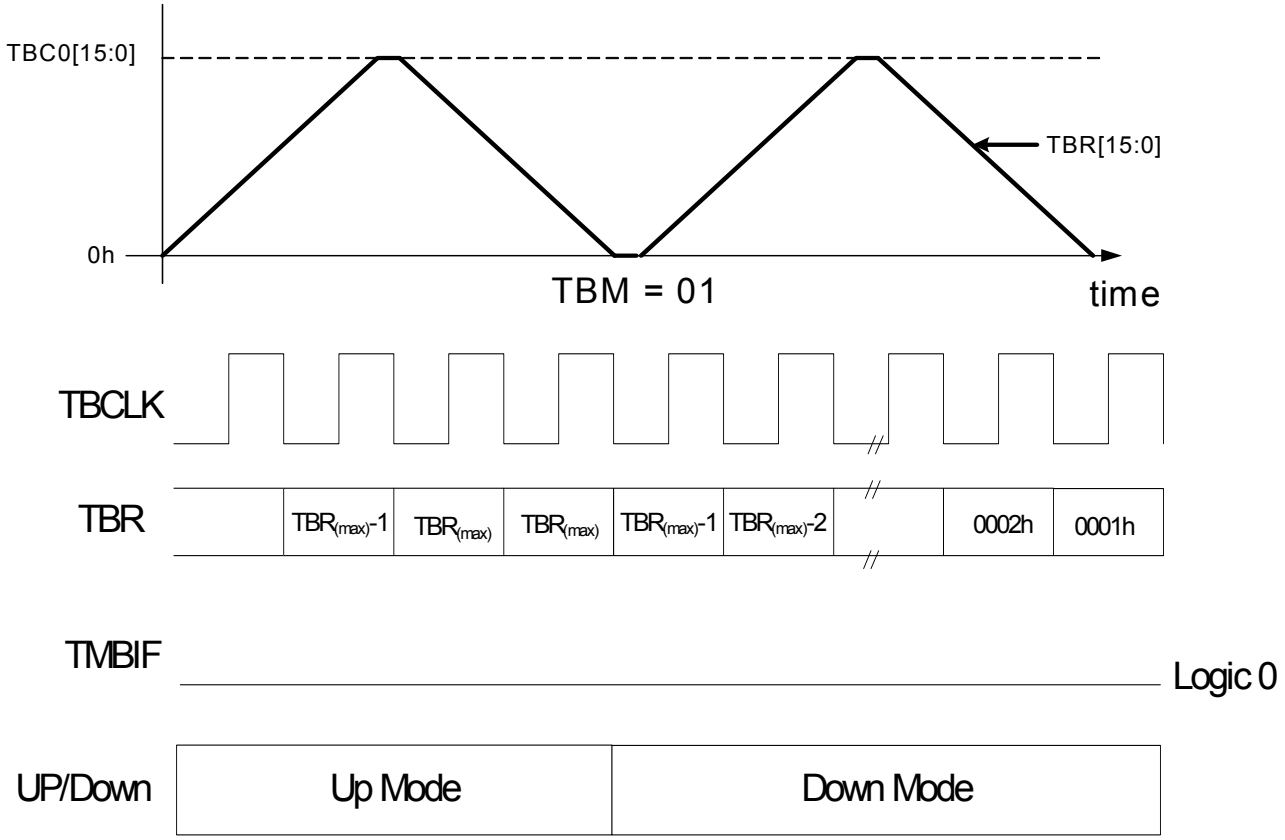
TMB counting method 1

When TBM [1:0] =01, the TMB will perform incremental counting and then perform decremental counting; the TBR is a 16-bit counter. After enabled, the TMB will perform incremental counting, and the TBR will automatically be added 1 at each rising edge of the TBCLK. When the TBR is equal to TBC0, the TBR will be changed to downward mode, but the interrupt flag TMBIF is still 0; at the next rising edge of the TBCLK, the TBR will be changed to perform decremental counting; the interrupt request will take place until the TBR is decreased to 0 and the interrupt flag TMBIF is set as <1>, and then the TBR will start to perform incremental counting at the next rising edge of the TBCLK. The above process will be kept repeating. The schematic view of the counting waveform of the mode is as shown in the following figure.

In the mode, the calculation method of the counting cycle of the TMB is:
T=2*TBC0*TMCD / HS_CK(or LS_CK)



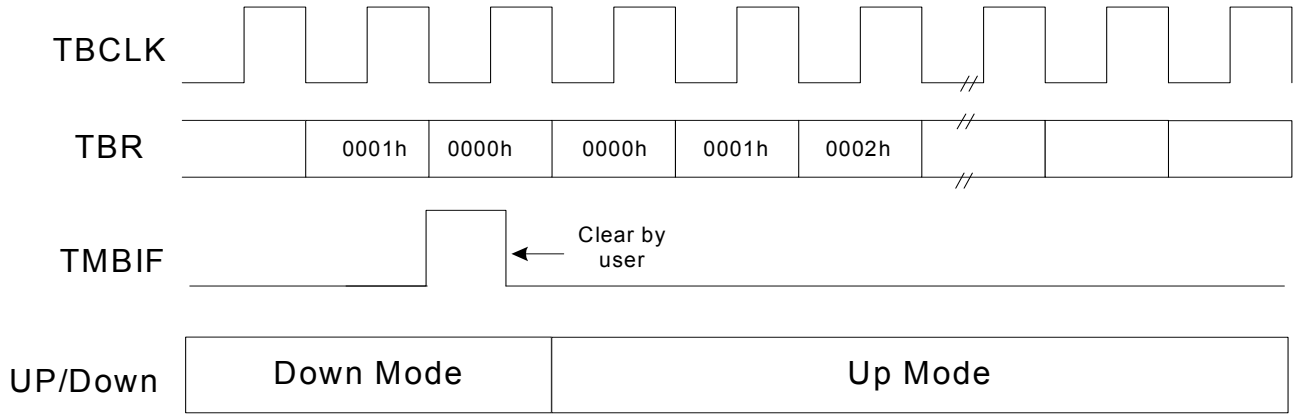


FIG. 10-3 Schematic view of counting waveform of counting method 1

TMB counting method 2

When TBM [1:0] =01, the TMB will perform incremental counting, but the TBR is separated into two independent 8-bit counters: TBR [15:8] and TBR [7:0]. Besides, the two independent 8-bit counters perform incremental counting at the same time. The overflow value of the TBR [15:8] is controlled by the TBC0 [15:8] and the overflow value of the TBR [7:0] is controlled by TBC0 [7:0]. The two counters will be automatically added by 1 at each rising edge of the TBCLK. If the TBR [15:8] is equal to the TBC0 [15:8], the TBR [15:8] will become 0 at the next rising edge of the TBCLK but the interrupt flag TMBIF is still 0; if the TBR [7:0] is equal to TBC0 [7:0], TBR [7:0] will become 0 at the next rising edge of the TBCLK and the interrupt flag TMBIF will be set as <1>. At this time, if the TMB interrupt function and the global interrupt enable function are enabled, the chip will reply to the TMB interrupt. Under the mode, the interrupt request is controlled by the counter TBR[7:0]; therefore, during the mode, please pay attention to set the value of the TBC0[7:0] in order to control the TMB interrupt vector. The schematic view of the counting waveform of the mode is as shown in the following figure.

In the mode, the calculation method of the counting cycle of the interrupt method of the mode is: T=TBC0[7:0]*TMCD / HS_CK(or LS_CK);

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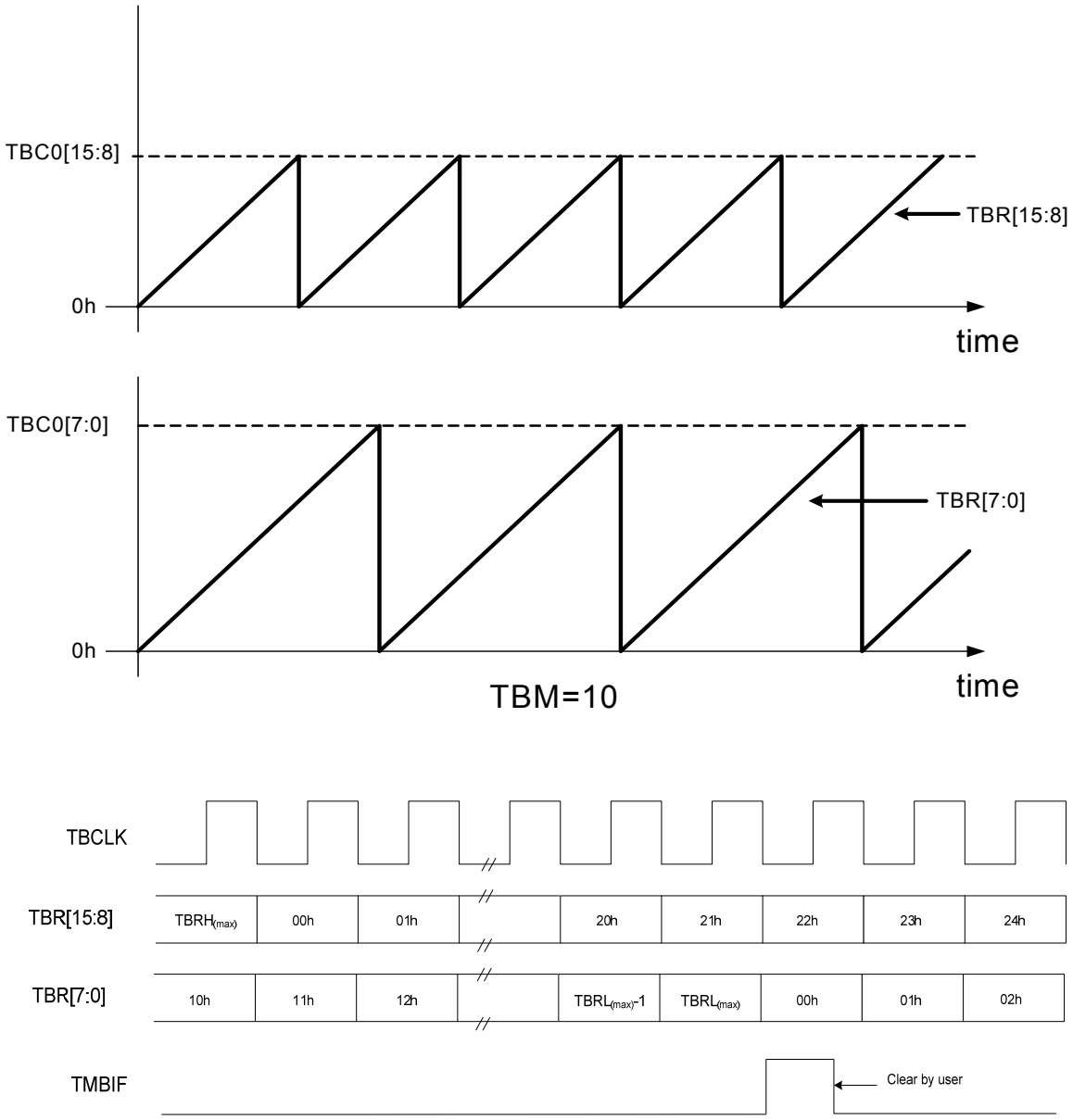

FIG. 10-4 Schematic view of counting waveform of counting method 2

TMB calculation method 3

When TBM [1:0] =11, the TMB will perform incremental counting, and the TBR is separated into two counters: TBR [15:8] and TBR [7:0]; and both of them are under incremental counting mode. The overflow value of the TBR [7:0] is controlled by the TBC0 [7:0] and the overflow value of the TBR [7:0] is controlled by TBC0 [7:0]. TBR [7:0] will be automatically added by 1 at each rising edge of the TBCLK; if the TBR [7:0] is equal to the TBC0 [7:0], the TBR will become 0 at the next rising edge of the TBCLK; besides the TMBIF will become 1 and the TBR [15:8] will be automatically added by 1. At this time, if the TMB interrupt function and the global interrupt enable function are enabled, the chip will reply to the TMB interrupt. The schematic view of the counting waveform of the mode is as shown in the following figure.

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In the mode, the calculation method of the counting cycle of the interrupt method of the mode is: T=TBC0[7:0]*TMCD / HS_CK(or LS_CK);

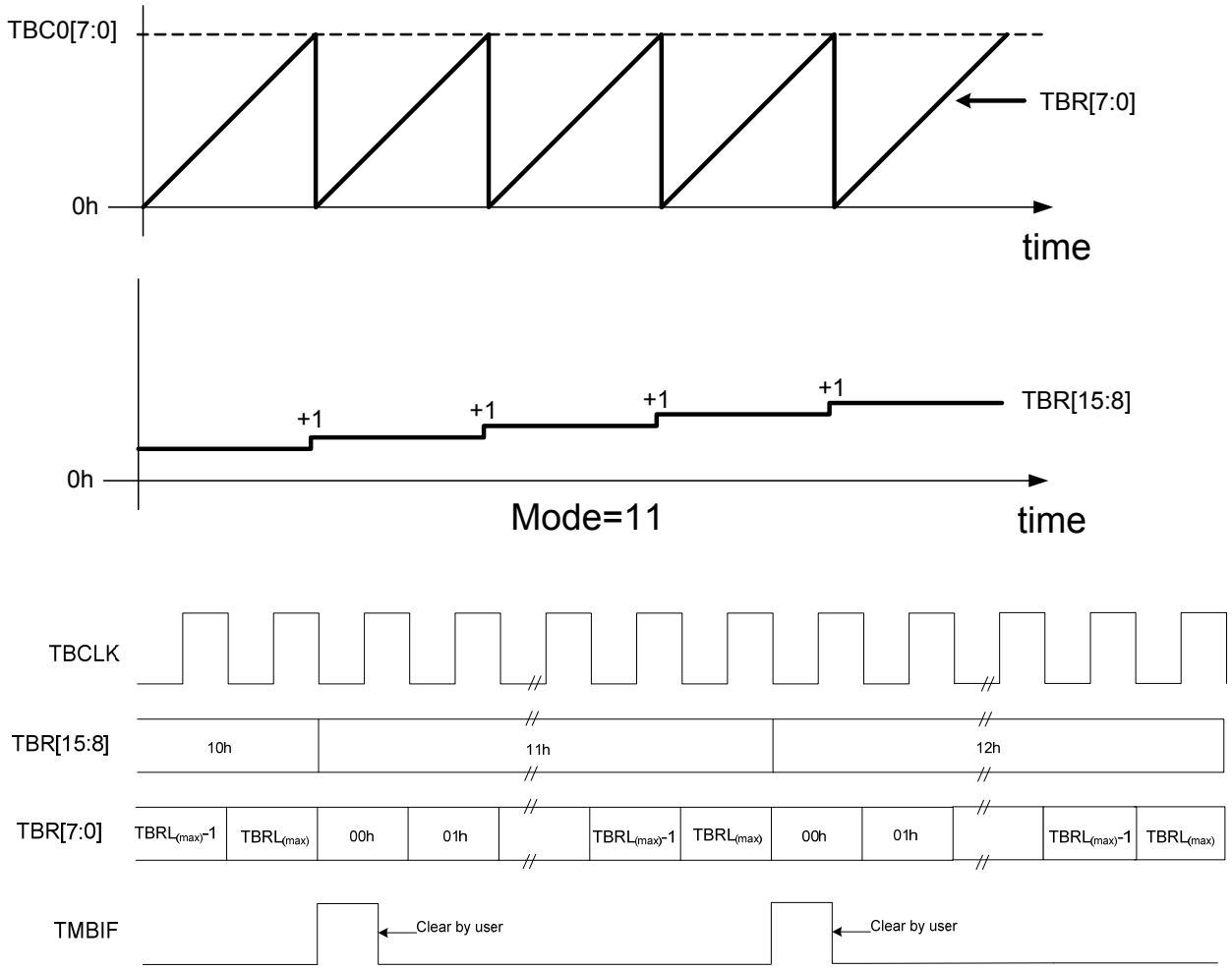

FIG. 10-5 Schematic view of counting waveform of counting method 3

10.1.2. PWM function mode

When the timer B works under the PWM mode, the combinations of the different counting methods and different PWM mode selectors can generate different PWM waveforms. The chip has only two PWMs: PWM0/PWM1, which can be simply considered two PWM waveform generators; the combinations of the different counting methods and different PWM operating modes can generate many kinds of PWM waveforms. The chip provides many output pins for the output of the PWM, and each PWM waveform generator is corresponding to 8 output IO ports; therefore, the usage and output of the PWM is very flexible. However, the TMB is necessary for the function; that is to say, the TMB should be enabled to set the counting cycle of the TMB.

Each of the PWM waveform generators (PWM0/PWM1) has many operating modes: PWMA, PWMB, PWMC, PWMD, PWME, PWMF and PWMG. The operating modes of the PWM0 and PWM1 can be changed by setting the control bits O0MD[2:0] and O1MD[2:1]. The phase of the output waveform of the PWM can be changed by setting the control bits O1PMR and O0PMR. The user can check the current operating mode of the PWM via the PWM operating mode flag register; if the flag is 1, it means the operating mode is enabled. The TBC1/TBC2 are the duty cycle controller of the PWM0/PWM1 respectively; the duty cycles of the PWMs can be changed by setting the values of the TBC1/TBC2.

The chip provides 8 output IOs for each PWM, and the corresponding pins are distributed over the PT1/PT2; the selection and enablement of the output pins of the PWM1 and PWM0 are controlled by the controllers PTPW[2:0], PTPW1E and PTTPW0E. The output and disablement of the PWMs can be controlled by the enablement and disablement of the output pins of the PWMs. If the user wants to completely disable the PWMs, it is necessary to disable the output pins of the TMB and the PWMs. The output pins of the PWMs are as shown in Table 10.1.

Serial number PTPW[2:0]	PWM0 Output pins	PWM1 Output pins	Serial number TPW[2:0]	PWM0 Output pins	PWM1 Output pins
000	PT1.0	PT1.1	100	PT2.0	PT2.1
001	PT1.2	PT1.3	101	PT2.2	PT2.3
010	PT1.4	PT1.5	110	PT2.4	PT2.5
011	PT1.6	PT1.7	111	PT2.6	PT2.7

Table 10-1 PWM output pin distribution

PWM operation description:

Set the operating clock frequency source of the TMB, and set the ENTD=1, TMCD[1:0]; Select the counting method and counting-trigger signal source of the TMB and set the control bits TBM and TBEBS;

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Set the counting cycle of the TMB and enable the TMB, which means TBEN=1 and writing value in TBC0;
Select the operating mode, duty cycle and output waveform phase of the PWM; that is to set O0MD/O0PMR and O1MD/O1PMR, and write values in TBC1/TBC2;
Select the output IO port of the PWM and the corresponding IO port should be set as the output mode; the enablement and disablement of the output IOs can control the output and disablement of the PWM; if the user wants to completely disable the PWMs, it is necessary to disable the TMB.

The waveform of the PWM is generated by the combination of the TBR, TBC0, TBC1 and TBC0; and there are 6 kinds of operating modes; thus, the operating conditions of the operating modes are different from each other. The 6 operating modes will be respectively specified later. The usage conditions and the controls of the two independent PWMs: PWMO0 and PWMO1; therefore, they will not be specified separately.

PWMA mode

The PWMA mode is a 16-bit PWM; the counting value of the TBR is compared with the TBC1 and the waveform period of the PWM is controlled by the TBC0.
PWM = 1, when TBR [15:0] >= TBC1 [15:0];
PWM = 0, when TBR [15:0] < TBC1 [15:0];

PWM period:

PWM Period = TBR[15:0]*TMCD / HS_CK(or LS_CK)；

PWM duty cycle:

PWM Duty= TBC1/(TBR[15:0]+1)
PWM Duty Cycle=（PWM Duty） *TMCD / HS_CK(or LS_CK)；

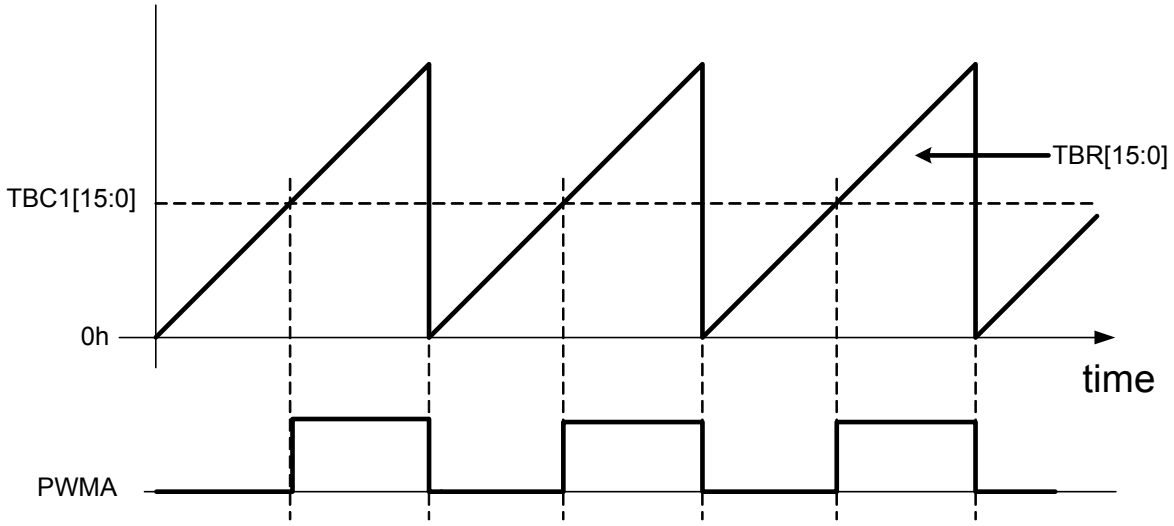

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FIG. 10-6　Waveform schematic view and counting waveform schematic view of PWM mode A

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PWMB mode

The PWMB mode is a 16-bit PWM; the counting value of the TBR is compared with the TBC2 and the waveform period of the PWM is controlled by the TBC0.

PWM = 1, when TBR [15:0] >= TBC2 [15:0];

PWM = 0, when TBR [15:0] < TBC2 [15:0];

PWM period:

PWM Period = TBR[15:0]*TMCD / HS_CK(or LS_CK);

PWM duty cycle:

PWM Duty= TBC2/(TBR[15:0]+1)

PWM Duty Cycle=(PWM Duty) *TMCD / HS_CK(or LS_CK);

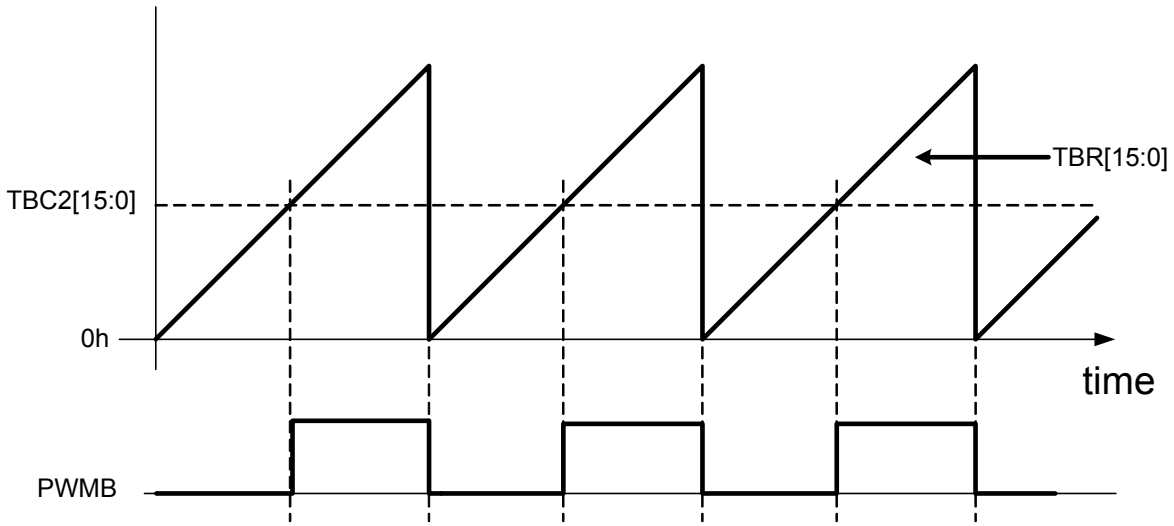

FIG. 10-7 Waveform schematic view and counting waveform schematic view of PWM mode B

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PWMC mode

The PWMC mode is a 8-bit PWM; the counting value of the TBR is compared with the TBC1[7:0] and many PWM waveforms appear within the period of the TBC0.

PWM output status control conditions:

PWM = 1, when TBR [7:0] >= TBC1 [7:0].

PWM = 0, when TBR [7:0] < TBC1 [7:0].

PWM period:

PWM Period = TBR[7:0]*TMCD / HS_CK(or LS_CK);

PWM duty cycle:

PWM Duty= TBC1[7:0]/(TBR[7:0]+1)

PWM Duty Cycle=(PWM Duty) *TMCD / HS_CK(or LS_CK);

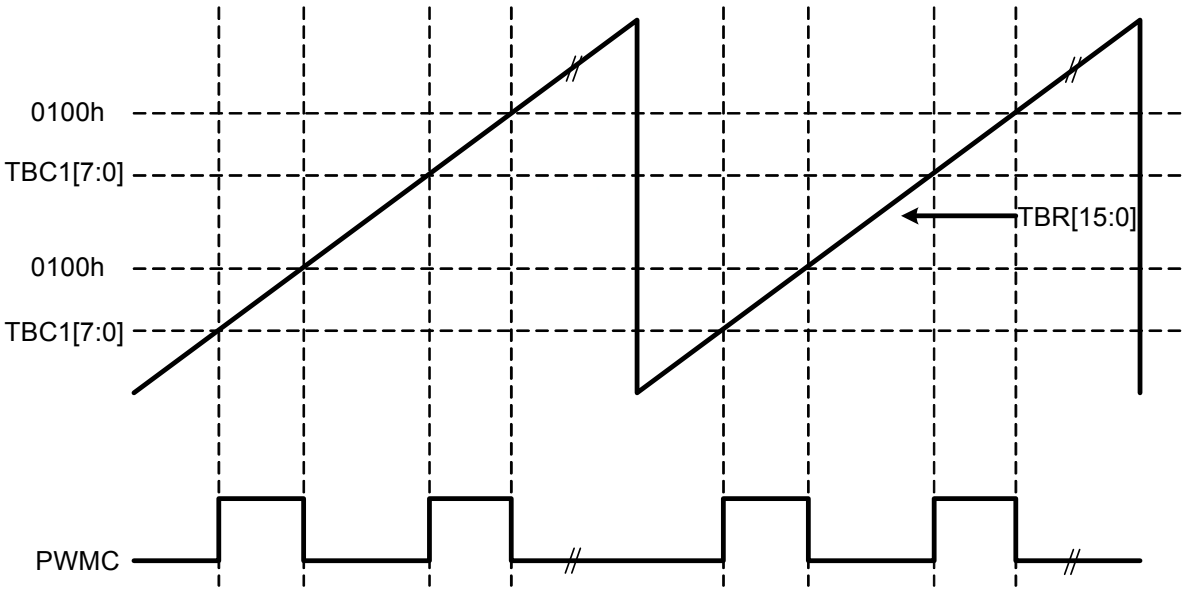

FIG. 10-8 Waveform schematic view and counting waveform schematic view of PWM mode C

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PWMD mode

The PWMC mode is a 8-bit PWM; the counting value of the TBR is compared with the TBC2[7:0] and many PWM waveforms appear within the period of the TBC0.

PWM output status control conditions:

PWM = 1, when TBR [15:8] >= TBC2 [7:0];

PWM = 0, when TBR[15:8] < TBC2[7:0];

PWM period:

PWM Period = TBR[15:8]*TMCD / HS_CK(or LS_CK);

PWM duty cycle:

PWM Duty= TBC2[7:0]/(TBR[15:8]+1)

PWM Duty Cycle=(PWM Duty) *TMCD / HS_CK(or LS_CK);

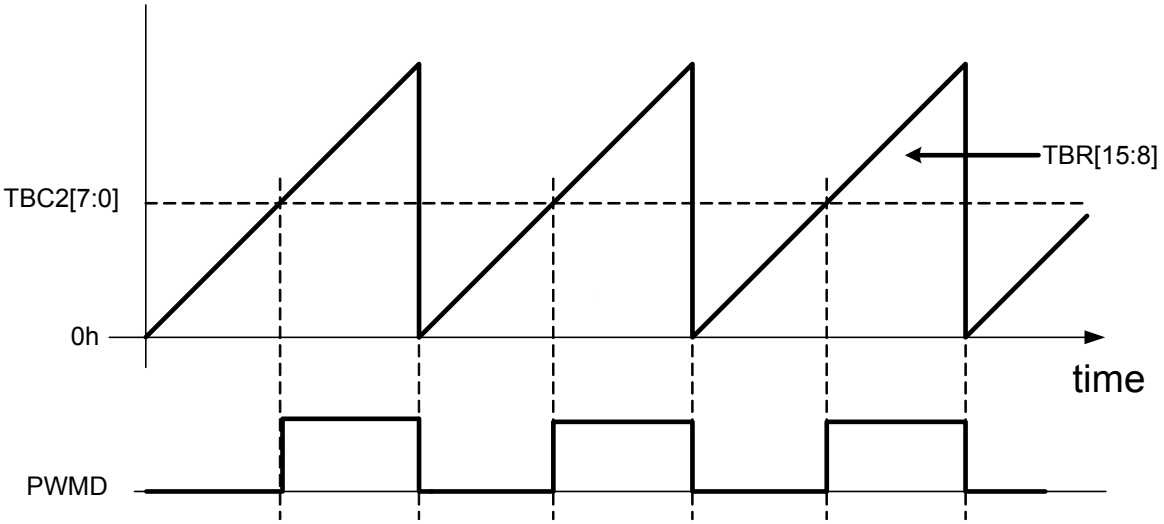

FIG. 10-9 Waveform schematic view and counting waveform schematic view of PWM mode D

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PWME waveform (8+8-bit PWM)

Set the TMB counter as the 8+8-bit mode and select the PWME as the output waveform of the PWM; then the 8+8bit PWM output is acquired.

The 8+8-bit PWM is composed of the control registers TBR[7:0], TBR[15:8], TBC0[7:0], TBC1[7:0] and TBC2[7:0], etc., and the internal digital circuits, where the TBR[7:0] is the accumulating counter, the TBC0[7:0] is the PWM frequency controller and when the counting of the TBR[7:0] reaches the TBC0[7:0], the TBR[15:8] will be added by 1; the TBC1[7:0] is the PWM duty cycle controller and the TBC2[7:0] is 8+8-bit PWM duty cycle adjuster.

(※The following waveform description is under the conditions that the O1PMR or O0PMR is set as <0> and outputs inversely)

The configuration and description of the 8+8-bit PWM duty cycle adjuster TBC2[7:0] are as shown in the follow table.

Configuration / Weighted quantity	TBC2[7:0]							
	01h	02h	04h	08h	10h	20h	40h	80h
PWM duty cycle fine adjustment	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
Description	TMB overflows 2 times; 1 is N+1, and 1 is N	TMB overflows 4 times; 3 are N, and 1 is N+1	TMB overflows 8 times; 7 are N, and 1 is N+1	TMB overflows 16 times; 15 are N, and 1 is N+1	TMB overflows 32 times; 31 are N, and 1 is N+1	TMB overflows 64 times; 63 are N, and 1 is N+1	TMB overflows 128 times; 127 are N, and 1 is N+11	TMB overflows 256 times; 255 are N, and 1 is N+1

Table 10-1 Configuration table of duty cycle adjuster

- The description of the duty cycle adjuster TBC2[7:0], where N is the width of the duty cycle (PS: *N = TBC1[7:0].*
  - Basic type
    - Set the TBC2[7:0] as 01h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 2 output periods as one set, where one outputs N and then the other one outputs N+1.
    - Set the TBC2[7:0] as 02h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 4 output periods as one set, where 3 of them continuously outputs N and the last one outputs N+1
    - Set the TBC2[7:0] as 04h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 8 output periods as one set, where 7 of them continuously outputs N and the last one outputs N+1.

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- Set the TBC2[7:0] as 08h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 16 output periods as one set, where 15 of them continuously outputs N and the last one outputs N+1
- Set the TBC2[7:0] as 10h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 32 output periods as one set, where 31 of them continuously outputs N and the last one outputs N+1
- Set the TBC2[7:0] as 20h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 64 output periods as one set, where 63 of them continuously outputs N and the last one outputs N+1
- Set the TBC2[7:0] as 40h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 128 output periods as one set, where 127 of them continuously outputs N and the last one outputs N+1
- Set the TBC2[7:0] as 80h, which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 256 output periods as one set, where 255 of them continuously outputs N and the last one outputs N+1

■ Logic calculation OR superposition type

(Only 1/2+1/4,1/2+1/8,~,1/2+1/4+1/8+1/16+1/32+1/64+1/128,1/2+1/4+1/8+1/16+1/32+1/64+1/256 are used to illustrated.)

- Set the TBC2[7:0] as 03h(1/2+1/4), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 4 output periods as one set, where one of them outputs N and then the other 3 output N+1.
- Set the TBC2[7:0] as 05h(1/2+1/8), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 8 output periods as one set, where 3 of them output N and then the other 5 output N+1.
- Set the TBC2[7:0] as 09h(1/2+1/16), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 16 output periods as one set, where 7 of them output N and then the other 9 output N+1.
- Set the TBC2[7:0] as 11h(1/2+1/32), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 32 output periods as one set, where 15 of them output N and then the other 17 output N+1
- Set the TBC2[7:0] as 21h(1/2+1/64), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 64 output periods as one set, where 31 of them output N and then the other 33 output N+1
- Set the TBC2[7:0] as 41h(1/2+1/128), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 128 output periods as one set, where 63 of them output N and then the other 67 output N+1

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- Set the TBC2[7:0] as 81h(1/2+1/256), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 256 output periods as one set, where 127 of them output N and then the other 129 output N+1
- Set the TBC2[7:0] as 07h(1/2+1/4+1/8), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 8 output periods as one set, where one of them outputs N and then the other 7 output N+1
- Set the TBC2[7:0] as 07h(1/2+1/4+1/8+1/16), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 16 output periods as one set, where one of them outputs N and then the other 15 output N+1.
- Set the TBC2[7:0] as 1Fh(1/2+1/4+1/8+1/16+1/32), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 32 output periods as one set, where one of them outputs N and then the other 31 output N+1
- Set the TBC2[7:0] as 3Fh(1/2+1/4+1/8+1/16+1/32+1/64), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 64 output periods as one set, where one of them outputs N and then the other 63 output N+1.
- Set the TBC2[7:0] as 7Fh(1/2+1/4+1/8+1/16+1/32+1/64+1/128), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 128 output periods as one set, where one of them outputs N and then the other 127 output N+1.
- Set the TBC2[7:0] as FFh(1/2+1/4+1/8+1/16+1/32+1/64+1/128+1/256), which makes the waveform of the PWM duty cycle generates the N+1 and N outputs, which is to generate a waveform using 256 output periods as one set, where one of them outputs N and then the other 255 output N+1.

◆ The following Table 10.2 and FIG. 10-10 list partial 8+8-bit PWM waveform changes under different configurations of the TBC2[7:0] for your reference.

8+8bit PWM			Overflowing times of TBN																		
型態	TBC2 [7:0]	邏輯運算	0	1	2	3	4	5	6	7	8	9	10	~	127	128	~	252	253	254	255
基本	01h	1/2	N	N+1	N	N+1	N	N+1	N	N+1	N	N+1	N	~	N+1	N	~	N	N+1	N	N+1
	02h	1/4	N	N	N+1	N	N	N	N+1	N	N	N	N+1	~	N	N	~	N	N	N+1	N

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波	04h	1/8	N	N	N	N	N+1	N	N	N	N	N	N	~	N	N	~	N+1	N	N	N
形	08h	1/16	N	N	N	N	N	N	N	N	N+1	N	N	~	N	N	~	N	N	N	N
	10h	1/32	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	20h	1/64	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	40hh	1/128	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	80h	1/256	N	N	N	N	N	N	N	N	N	N	N	~	N	N+1	~	N	N	N	N
邏	03h	3/4	N	N+1	N+1	N+1	N	N+1	N+1	N+1	N	N+1	N+1	~	N+1	N	~	N	N+1	N+1	N+1
輯	05h	5/8	N	N+1	N	N+1	N+1	N+1	N	N+1	N	N+1	N	~	N+1	N	~	N+1	N+1	N	N+1
運	07h	7/8	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	N+1	N	~	N+1	N	~	N+1	N+1	N+1	N+1
算	0Fh	15/16	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	~	N+1	N	~	N+1	N+1	N+1	N+1
疊	85h	161/256	N	N+1	N	N+1	N+1	N+1	N	N+1	N	N+1	N	~	N+1	N+1	~	N+1	N+1	N	N+1
何	8Fh	241/256	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	~	N+1	N+1	~	N+1	N+1	N+1	N+1
形	FFh	255/256	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	~	N+1	N+1	~	N+1	N+1	N+1	N+1

Table 10-2　PWME output waveform table

型態 Type

邏輯運算 Logic calculation

基本波形 Basic waveform

邏輯運算疊合波形 Logic calculation superposition waveform

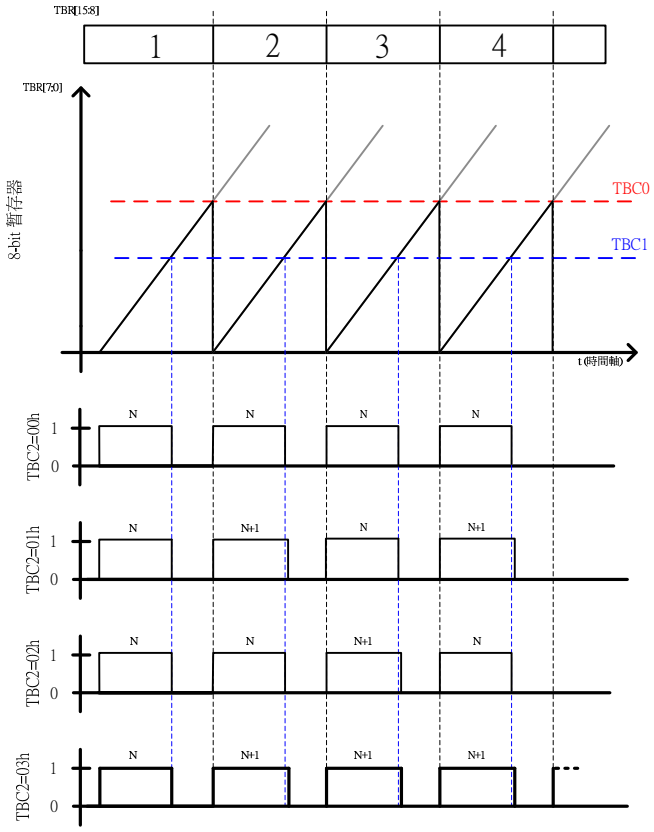

FIG. 10-10 Schematic view of PWME output waveforms

PWME output operation description

- Initialization (The PWM frequency and duty cycle configuration)
  - Setting the TMCKS[0] can select the operating frequency source of the TMB, and setting the TMCD[1:0] can determine the operating frequency of the TMB.
  - When the TBM[1:0 is set as <11>, the TMB serves as 8+8-bit counter.
  - When the O0MD[2:0] or O1MD[2:0] is set as <100>, the output waveform is the PWME.
  - Setting the TBEBS[1:0] as <00> can set the counting-trigger signal as “Always Enable”, which means cycle counting
  - Write data in the TBC0[7:0] to determine the frequency of the PWM.
  - Write data in the TBC1[7:0] to determine the duty cycle of the PWM.
  - Write data in the TBC2[7:0] to determine the duty cycle fine adjustment method of the PWM.
  - Setting the TBEN[0] as <1> to enable the counter.
- Generate PWME waveform
  - When the counting value of the TBR[7:0] is equal to that of the TBC1[7:0], the PWME will be 0➔1.
  - When the counting value of the TBR[7:0] is equal to that of the TBC0[7:0] again, the PWME will be 1➔0；
    - ✓ And the overflowing event takes place to set the TBxIF[0] as <1> , and reset and restart the incremental counting; at this time, if the TBxIE[0]] is set as<1>, the interrupt event service will take place.
    - ✓ At this time, the set value of the TBC2[7:0] adjusts the outputs of the PWME to be N+1 and N, as shown in the table, where N＝TBC1[7:0].
- PWM output control
  - Set the O0PMR[0] or O1PMR[0] to determine whether the output waveform of the pins is opposite in phase or not.
    Set the PTPW0E[0] or PTPW1E[1] as <1> to set the pin of the PWM waveform be under output status select appropriate PWM waveform output pin for the PTPW[2:0].
- Set the TBEN[0] as <0> to disable the counter and the PWM output.
- The calculation formula of the frequency and duty cycle of the PWME:

$$D = \frac{TBC1 + \frac{微調}{256}}{TBC0 + 1}$$

Fine adjustment

  - Fine adjustment is effective when the duty cycle is N+1; the formula is as follows:
    <X>stands for each bit of the TBC2.

$$微調 = <0> * 128 + <1> * 64 + <2> * 32 + <3> * 16 + <4> * 8 + <5> * 4 + <6> * 2 + <7>$$

Fine adjustment

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PWMF mode

The PWMF is a 16-bit PWM. The counting value of the TBR is compared with the TBC1 and TBC2, and the TBC2 should be larger than TBC1; the TBR will keep increasing until overflowing.

PWM output status control conditions:

PWM = 1, when TBC1[15:0] =< TBR[15:0] <= TBC2[15:0];

PWM = 0, when TBR[15:0] > TBC2[15:0] or TBR[15:0] <= TBC1[15:0];

PWM=1; the time is: t = tclock × (TBC2 – TBC1);

PWM period:

PWM Period = TBR[15:0]*TMCD / HS_CK(or LS_CK);

PWM duty cycle:

PWM Duty= (TBC2-TBC1)/(TBR[15:0]+1)

PWM Duty Cycle=(PWM Duty) *TMCD / HS_CK(or LS_CK);

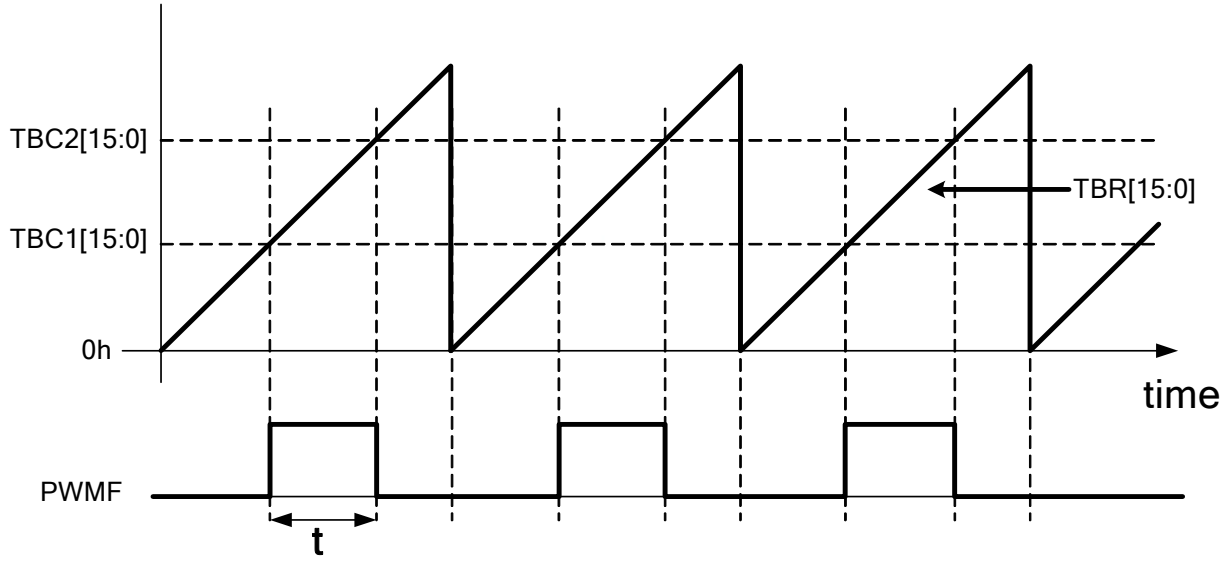

FIG. 10-10 Waveform schematic view and counting waveform schematic view of PWM mode F

PWMG mode

The PWMG is a 16-bit PWM mode and the duty cycle of the output waveform is 50%, which is the PFD waveform. The counting value of the TBR is not compared with the TBC1/TBC2, and the period of the output waveform is related to the TBC0.

PWM period:

PWM Period = TBC0[15:0]*TMCD / HS_CK(or LS_CK);

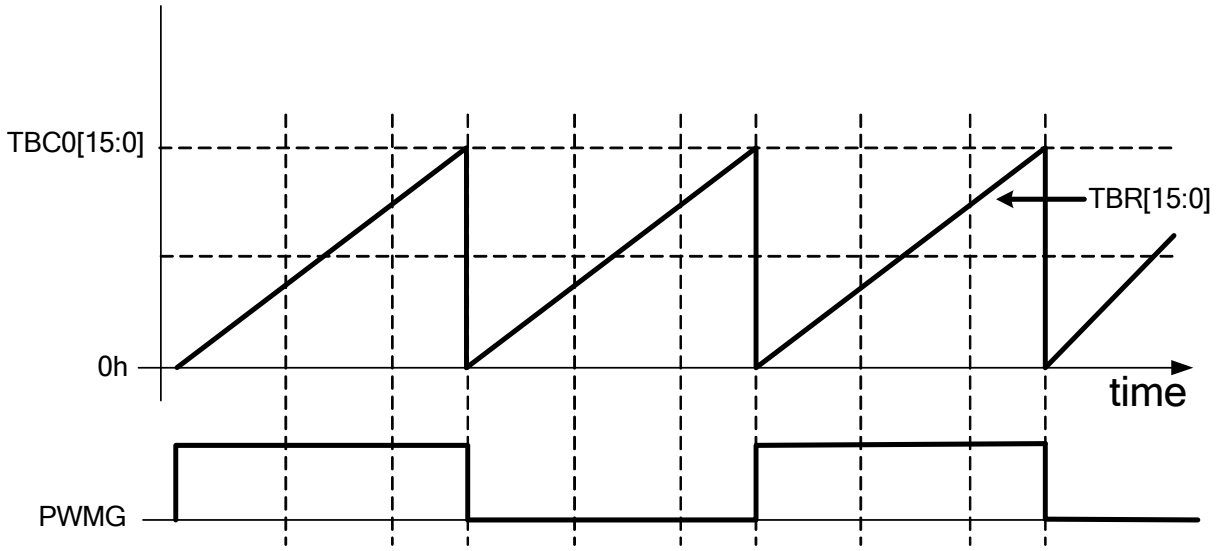

FIG. 10-11 Waveform schematic view and counting waveform schematic view of PWM mode G

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10.2. Register address

TMB Register Address	31	24	23	16	15	8	7	0
TMA Base Address + 0x04(0x40C04)	MASK1		REG1		MASK0		REG0	
TMA Base Address + 0x08(0x40C08)	-		REG2		TBCR		TBCR	
TMA Base Address + 0x0C(0x40C0C)	-		-		TBC0		TBC0	
TMA Base Address + 0x10(0x40C10)	TBC2		TBC2		TBC1		TBC1	

- Reserved

10.3. Register function

10.3.1. Timer B register TMBCR0

TMA Base Address + 0x04 (0x40C04)							
Symbol	TMBCR0(TMB Control Register 0)						
Bit	[31:24]	[23]	[22:20]		[19]		[18:16]
Name	MASK	O1PMR	O1MD		O0PMR		O0MD
RW	R0W-0	RW-0					
Bit	[15:8]	[7]	[6]	[5]	[4]	[3:2]	[1:0]
Name	MASK	-	Reg	TBEN	TBRST	TBM	TBEBS
RW	R0W-0	-	RW-0				

Bit	Name	Description	
Bit[23]	O1PMR	PWM1 waveform output phase control	
		0	Inverted output
		1	Normal output
Bit[21-20]	O1MD	PWM1 operating mode selection	
		000	PWMA
		001	PWMB
		010	PWMC
		011	PWMD
		100	PWME
		101	PWMF
		110	PWMG
		111	PWMG
Bit[19]	O0PMR	PWM0 waveform output phase control	
		0	Inverted output
		1	Normal output
Bit[18-16]	O0MD	PWM0 operating mode selection	
		000	PWMA
		001	PWMB

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		010	PWMC
		011	PWMD
		100	PWME
		101	PWMF
		110	PWMG
		111	PWMG
Bit[5]	TBEN	Timer B enablement control	
		0	Disable
		1	Enable
Bit[4]	TBRST	Timer B reset	
		0	Normal
		1	Clear the counting register TBR of the Timer B; it will be automatically set as 0 after finished.
Bit[3~2]	TBM	Timer B counting mode selection	
		00	16-bit up counter; sawtooth-wave type counting method; the counting will increase to the maximum TBC0 on the basis that the step is 1.
		01	16-bit up/down counter; triangle-wave type counting method; the counting will increase to the maximum TBC0 on the basis that the step is 1 and then decrease to 0.
		10	2 independent 8-Bit up counters TBR[15:8] and TBR[7:0]; sawtooth-wave type counting method; the two counters will increase to the maximums TBC0[15:8] and TBC0[7:0] at the same time on the basis that the step is 1.
		11	2 8-Bit up counters TBR[15:8] and TBR[7:0], sawtooth-wave type counting method with step being 1; after the counter TBR[7:0] increases and then overflows, the counter TBR[15:8] is automatically added by 1 and then the TBR[7:0] restarts the counting from 0.
Bit[1~0]	TBEBS	Timer B counting-trigger mode selection	
		00	1 Always enable, continuous counting method
		01	CMPO trigger the multi-function comparator to output high potential
		10	OPOD trigger the OP amplifier to output high potential
		11	CPI1 trigger the output of the Timer C CPI1 to output high potential

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10.3.2. Timer B register TMBCR1

TMA Base Address + 0x08 (0x40C08)							
Symbol	TMBCR1(TMB Control Register 1)						
Bit	[31:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	-	PWMF	PWME	PWMD	PWMC	PWMB	PWMA
RW	-	R-X					
Bit	[15:0]						
Name	Timer B counting value						
RW	R-X						

Bit	Name	Description	
Bit[21-16]	PWM Flag	PWM A/B/C/D/F operating mode status flag	
		0	Normal
		1	Enable
Bit[15-0]	TMBC	Timer B 16-bit counting value	

10.3.3. Timer B register TMBCOD

TMA Base Address + 0x0C (0x40C0C)	
Symbol	TMBCOD(TMB Counter overflow condition Register)
Bit	[31:16]
Name	-
RW	-
Bit	[15:0]
Name	TBC0:Timer B Overflow Condition
RW	RW-0xFFFF

Bit	Name	Description
Bit[15-0]	TBC0	Timer B counter overflow threshold value

10.3.4. Timer B register PWMDOD

TMA Base Address + 0x10 (0x40C10)	
Symbol	PWMDOD(PWM counter overflow condition Control Register)
Bit	[31:16]
Name	TBC2: PWM1 duty cycle counter overflow value
RW	RW-FFFFh
Bit	[15:0]
Name	TBC1: PWM0 duty cycle counter overflow value
RW	RW-FFFFh

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Bit	Name	Description
Bit[31-16]	TBC2	PWM1 duty cycle counter overflow value
Bit[15-0]	TBC1	PWM0 duty cycle counter overflow value

10.4. Model program flow

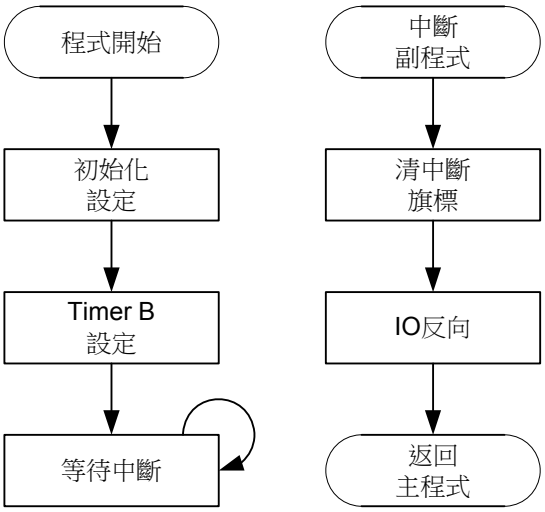
The HYCON C Library is adopted; the DrvTMBC_Clk_Source(X,Y) can select the clock source of the Timer B; X can select the high speed or low speed; X=0 is HS_CK; Y is the frequency dividing selection; if Y=3., it means the Timer B IP clock and the frequency dividing is 8.

The function DrvTMB_Open(E_TMB_MODE0,E_TMB_NORMAL,0xFFFF) means the TimerB IP settings, including the Mode selection, the Timer B enablement and the Timer B counter counting settings.

The HYCON C Library DrvTIMER_EnableInt(E_TMB) means enabling the Timer B interrupt.

The HYCON C Library DrvTIMER_ClearIntFlag(E_TMB) means clearing the TimerB interrupt flag.

The Timer A/B/C and WDT belong to the HW1 interrupt and the format is void HW1_ISR(void).



The program starts.

Initialization settings

Timer B settings

Wait for interrupt

Interrupt the subprogram

Clear the interrupt flag

Reverse the I/O

Return to the main program

10.5. Model program function

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Use the TimerB interrupt.

Each TimerB interrupt will reverse the IO.

Ex: it is 0x5 before the interrupt; it will become 0xA after the interrupt.

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10.6 Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int i;
04
05  int main(void)
06  {
07      i=0x05;
08      DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);          //PT2_0~3 Set Output
09      DrvGPIO_SetPortBits(E_PT2,i);                  //PT2 Output i=0x05
10
11      DrvTMBC_Clk_Source(0,3);                       //Timer B Prescaler 1
12                                                     //0: HS_CK,clock source.
13                                                     //3: clock divider.÷8
14
15      DrvTMB_Open(E_TMB_MODE0,E_TMB_NORMAL,0xFFFF);  //Timer B overflow 0xFFFF
16      DrvTIMER_ClearIntFlag(E_TMB);                  //Clear TMB interrupt flag
17      DrvTIMER_EnableInt(E_TMB);                     //Timer B interrupt enable
18
19      SYS_EnableGIE(7);                              //Enable GIE
20
21      while(1);                                      //Wait for Interrupt
22  }
23
24  void HW1_ISR(void)
25  {
26      DrvTIMER_ClearIntFlag(E_TMB);                  //Clear TMB interrupt flag
27      i=i^0xF;                                       //i XOR 0xF
28      DrvGPIO_SetPortBits(E_PT2,i);                  //PT2 Output i=0x0A~0x05
29  }
30
```

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11. TIMER B2

11.1. Register address

TMB2 Register Address	31 24	23 16	15 8	7 0
TMA Base Address + 0x24(0x40C24)	MASK1	REG1	MASK0	REG0
TMA Base Address + 0x28(0x40C28)	-	REG2	TB2CR	TB2CR
TMA Base Address + 0x2C(0x40C2C)	-	-	TB2C0	TB2C0
TMA Base Address + 0x30(0x40C30)	TB2C2	TB2C2	TB2C1	TB2C1

11.2. Register function

11.2.1. Timer B2 register TMB2CR0

TMA Base Address + 0x24 (0x40C24)							
Symbol	TMB2CR0(TMB2 Control Register 0)						
Bit	[31:24]	[23]	[22:20]		[19]	[18:16]	
Name	MASK	O3PMR	O3MD		O2PMR	O2MD	
RW	R0W-0	RW-0					
Bit	[15:8]	[7]	[6]	[5]	[4]	[3:2]	[1:0]
Name	MASK	-	Reg	TB2EN	TB2RST	TB2M	TB2EBS
RW	R0W-0	-	RW-0				

Bit	Name	Description	
Bit[23]	O3PMR	PWM3 waveform output phase control	
		0	Inverted output
		1	Normal output
Bit[21-20]	O3MD	PWM3 operating mode selection	
		0	PWMA
		1	PWMB
		2	PWMC
		3	PWMD
		4	PWME
		5	PWMF
		6	PWMG
		7	PWMG
Bit[19]	O2PMR	PWM2 waveform output phase control	
		0	Inverted output
		1	Normal output
Bit[18-16]	O2MD	PWM2 operating mode selection	
		0	PWMA
		1	PWMB

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		2	PWMC
		3	PWMD
		4	PWME
		5	PWMF
		6	PWMG
		7	PWMG
Bit[5]	TB2EN	Timer B2 enablement control	
		0	Disable
		1	Enable
Bit[4]	TB2RST	Timer B2 reset	
		0	Normal
		1	Clear the counting register TBR of the Timer B; it will be automatically set as 0 after finished.
Bit[3~2]	TB2M	Timer B2 counting mode selection	
		00	16-bit up counter; sawtooth-wave type counting method; the counting will increase to the maximum TBC0 on the basis that the step is 1.
		01	16-bit up/down counter; triangle-wave type counting method; the counting will increase to the maximum TBC0 on the basis that the step is 1 and then decrease to 0.
		10	2 independent 8-Bit up counters TBR[15:8] and TBR[7:0]; sawtooth-wave type counting method; the two counters will increase to the maximums TBC0[15:8] and TBC0[7:0] at the same time on the basis that the step is 1.
		11	2 8-Bit up counters TBR[15:8] and TBR[7:0], sawtooth-wave type counting method with step being 1; after the counter TBR[7:0] increases and then overflows, the counter TBR[15:8] is automatically added by 1 and then the TBR[7:0] restarts the counting from 0.
Bit[1~0]	TB2EBS	Timer B2 counting-trigger mode selection	
		00	1 Always enable, continuous counting method
		01	CMPO trigger the multi-function comparator to output high potential
		10	OPOD trigger the OP amplifier to output high potential
		11	CPI1 trigger the output of the Timer C CPI1 to output high potential

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11.2.2. Timer B2 register TMB2CR1

TMA Base Address + 0x28 (0x40C28)							
Symbol	TMB2CR1(TMB Control Register 1)						
Bit	[31:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	-	PWMF	PWME	PWMD	PWMC	PWMB	PWMA
RW	-	R-X					
Bit	[15:0]						
Name	Timer B2 counting value						
RW	R-X						

Bit	Name	Description	
Bit[21-16]	PWM Flag	PWM A/B/C/D/F operating mode status flag	
		0	Normal
		1	Enable
Bit[15-0]	TMBC	Timer B2 16-bit counting value	

11.2.3. Timer B2 register TMB2COD

TMA Base Address + 0x2C (0x40C2C)	
Symbol	TMB2COD(TMB Counter overflow condition Register)
Bit	[31:16]
Name	-
RW	-
Bit	[15:0]
Name	TB2C0:Timer B Overflow Condition
RW	RW-0xFFFF

Bit	Name	Description
Bit[15-0]	TB2C0	Timer B2 counter overflow threshold value

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11.2.4. Timer B2 register PWM2DOD

TMA Base Address + 0x30 (0x40C30)	
Symbol	PWM2DOD(PWM counter overflow condition Control Register)
Bit	[31:16]
Name	TB2C2: PWM3 duty cycle counter overflow value
RW	RW-FFFFh
Bit	[15:0]
Name	TB2C1: PWM2 duty cycle counter overflow value
RW	RW-FFFFh

Bit	Name	Description
Bit[31-16]	TB2C2	PWM3 duty cycle counter overflow value
Bit[15-0]	TB2C1	PWM2 duty cycle counter overflow value

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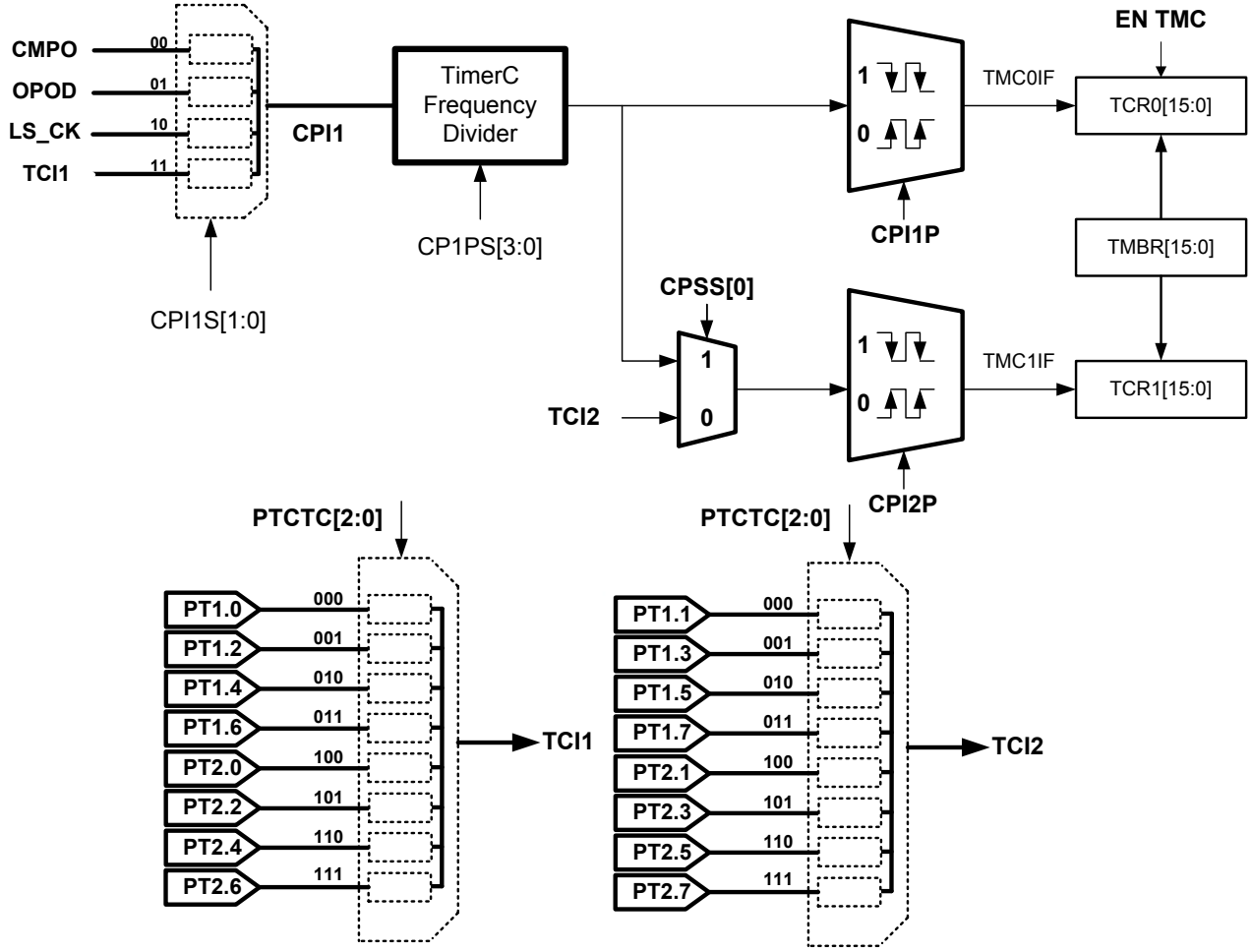
12. TIMER C

12.1. Overall description

The timer C is designed to execute the capture function, which can be used to perform frequency measurement, event counting, interval time measurement, etc. It can generate the interrupt signal when the counter overflow takes place; and it should be used together with the TMB counter register.



CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

Fig. 12-1 TC function block diagram

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TMC clock source

The clock source of the TMC is equal to that of the TMB; all of them are generate by make the HS_CK or LS_CK pass the frequency divider to generate the clock source TMBCLK. The capture function of the TMC can be enabled or disabled by setting the control bit TCEN[0].

TMC capture counting value

The capture counting value of the TMC is finished by the counter TBR of the TMB. When the TMC captures the first trigger edge of the input signal, the TBR will start the counting; when the TMC captures the second trigger edge of the input signal, the TBR will stop the counting. After the capture event is finished, the hardware will automatically write the value of the TBR into the TMCR1 or TMCR2, and generate the interrupt flags TMC1IF and TMC2IF. The user can read the values of the TCR1/TCR2 by program.

Capture comparator 1

The capture comparator 1 has four capture signal input sources, and the input signal source can be set by setting the selector CPI1S[1:0]; and the input signal should further pass the frequency divider C1PS[3:0]; the frequency divider can perform the frequency dividing on the input signal to slow the input signal; in this way, the input signals with high frequency can be measured. The setting of the controller TCPI1P can determine the trigger edge of the capture signal is the rising edge or the falling edge. After the capture event is finished, the interrupt signal can be generated and the interrupt flag TMC1IF is set as <1>.

The capture signal input source of the capture comparator 1:

Input signal source symbol	Function description
CMPO	The output status of the comparator
OPOD	The output status of the OP amplifier
LS_CK	Chip low-speed frequency source
TCI1	Input from the IO

The input of the capture comparator 1

Serial number	TCI1	TCI2	Serial number	TCI1	TCI2
000	PT1.0	PT1.1	100	PT2.0	PT2.1
001	PT1.2	PT1.3	101	PT2.2	PT2.3
010	PT1.4	PT1.5	110	PT2.4	PT2.5
011	PT1.6	PT1.7	111	PT2.6	PT2.7

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Operation of capture comparator 1:

Select the operating clock source TMBCLK of the TMC;

Set the capture signal input source and the input signal source frequency dividing value, which is to set the values of the CPI1S[1:0] and C1PS[3:0];

Set the capture signal trigger edge, which is to set the value of the TCPI1P;

If the TCI1 is selected to be the capture signal input source, it is necessary to set the input IO to select the corresponding IO as the input mode;

If the interrupt function is used, it is necessary to enable TMC0IE=1 and enable the global interrupt function GIE=1;

Enable the TMC and enable the TCEN.

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Capture comparator 2

The capture comparator 2 has 2 capture signal input sources, and the input signal source can be set by setting the selector CPI2S[0]; and the input signal does not have to pass the frequency divider. The setting of the controller TCPI2P can determine the trigger edge of the capture signal is the rising edge or the falling edge. After the capture event is finished, the interrupt signal can be generated and the interrupt flag TMC2IF is set as <1>.
The capture signal input of the capture comparator 2 is:
Input from IO port;
It is consistent with the input source of the capture comparator 1;

Operation of the capture comparator 2:
Select the operating clock source TMBCLK of the TMC;
Set the capture signal input source, which is to set the values of the CPI2S[0];
Set the capture signal trigger edge, which is to set the value of the TCPI2P;
If the TCI2 is selected to be the capture signal input source, it is necessary to set the input IO to select the corresponding IO as the input mode;
If the interrupt function is used, it is necessary to enable TMC1IE=1 and enable the global interrupt function GIE=1;
Enable the TMC and enable the TCEN.

12.2. Register address

TMC Register Address	31 24	23 16	15 8	7 0
TMA Base Address + 0x14(0x40C14)	MASK1	REG1	MASK0	REG0
TMA Base Address + 0x18 (0x40C18)	TCR2	TCR2	TCR1	TCR1

12.3. Register function

12.3.1. 1Timer C register TMCCR0

TMA Base Address + 0x14 (0x40C14)							
Symbol	TMCCR0(TMC Control Register 0)						
Bit	[31:24]	[23]	[22]	[21:20]	[19:16]		
Name	MASK	CPI1R	CPSS	CPI1S	CP1PS		
RW	R0W-0	RW-0					
Bit	[15:08]	[7:3]			[2]	[1]	[0]
Name	MASK	-			TCPI2P	TCPI1P	TCEN
RW	R0W-0	-			RW-0		

Bit	Name	Description
Bit[23]	CPI2R	Timer B TC1 input mode control

		0	Level trigger
		1	Rising edge trigger
Bit[22]	CPI2S	Capture 1 input signal source selection	
		0	The input of the TC2 from the IO port
		1	The input source the same with the capture 1
Bit[21~20]	CPI1S	Capture 0 input signal source selection	
		00	CMPO comparator output
		01	OPOD OP amplifier output
		10	Low-frequency clock LS_CK
		11	The input of the TC1 from the IO port
Bit[19~16]	C1PS	The frequency divider configuration of the input signal of the Capture1	
		0000	CPI1 frequency/1
		0001	CPI1 frequency/2
		0010	CPI1 frequency/4
		0011	CPI1 frequency/8
		0100	CPI1 frequency/16
		0101	CPI1 frequency/32
		0110	CPI1 frequency/64
		0111	CPI1 frequency/128
		1000	CPI1 frequency/256
		1001	CPI1 frequency/512
		1010	CPI1 frequency/1024
		1011	CPI1 frequency/2048
		1100	CPI1 frequency/4096
		1101	CPI1 frequency/8192
		1110	CPI1 frequency/16384
		1111	CPI1 frequency/32768
Bit[02]	TCPI2P	Capture2 trigger edge configuration	
		0	Rising edge trigger
		1	Falling edge trigger
Bit[01]	TCP1P	Capture1 trigger edge configuration	
		0	Rising edge trigger
		1	Falling edge trigger
Bit[00]	TCEN	Timer C enablement control	
		0	Disable (but the TCR0 and TCR1 are not cleared)
		1	Enable

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12.3.2. Timer C register TMCCR1

TMA Base Address + 0x18 (0x40C18)	
Symbol	TMCCR1(TMC Control Register 1)
Bit	[31:16]
Name	TCR2
RW	R-X
Bit	[15:00]
Name	TCR1
RW	R-X

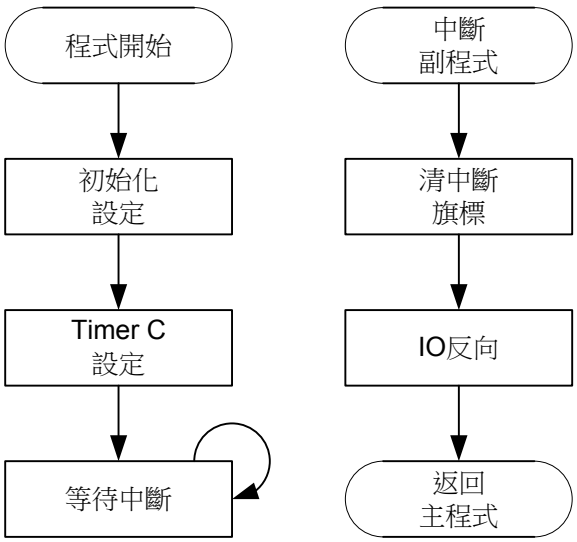
Bit	Name	Description
Bit[31-16]	TCR2	Capture2 frequency capture counter
Bit[15-00]	TCR1	Capture1 frequency capture counter

12.4. Model program flow

DrvTMB_Open( ) will enable the Timer B.

DrvCapture1_Open( ); set Timer C0.

DrvCapture2_Open( ); set Timer C1.



The program starts.

Initialization settings

Timer C settings

Wait for interrupt

Interrupt the subprogram

Clear the interrupt flag

Reverse the I/O

Return to the main program

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12.5. Model program function

Use the Timer C interrupt.

Each the Timer C interrupt will reverse the IO.

Ex: it is 0x5 before the interrupt; it is 0xA after the interrupt.

12.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int i;
04
05  int main(void)
06  {
07      i=0x05;
08      DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);          //PT2_0~3 Set Output
09      DrvGPIO_SetPortBits(E_PT2,i);                  //PT2 Output i=0x05
10
11      DrvTMBC_Clk_Source(0,0);                       //Timer B Prescaler 1
12                                                     //0: HS_CK,clock source.
13                                                     //0: clock divider.÷1
14
15      DrvTMB_Open(E_TMB_MODE0,E_TMB_NORMAL,0xFFFF); //Timer B overflow 0xFFFF
16
17      DrvCapture1_Open(2,14,1);                      //TimerC0 use as Capture 1
18                                                     //input source selection
19                                                     //2:LS_CK
20                                                     //14:÷16384 1:Positive-edge trigger
21
22      DrvCapture2_Open(1,1);                         //TimerC1 use as Capture 2
23                                                     // input source selection
24
25      DrvTIMER_ClearIntFlag(E_TMC0);                 //Clear TMC0 interrupt flag
26      DrvTIMER_ClearIntFlag(E_TMC1);                 //Clear TMC1 interrupt flag
27
28      DrvTIMER_EnableInt(E_TMC0);                    //TimerC0 interrupt enable
29      DrvTIMER_EnableInt(E_TMC1);                    //TimerC1 interrupt enable
30
31      SYS_EnableGIE(7);                              //Enable GIE
32
33      while(1);                                      //Wait for Interrupt
34  }
37
38  void HW1_ISR(void)
39  {
40      DrvTIMER_ClearIntFlag(E_TMC0);                 //Clear TMC0 interrupt flag
41      DrvTIMER_ClearIntFlag(E_TMC1);                 //Clear TMC1 interrupt flag
42      i=i^0xF;                                       //i XOR 0xF
43      DrvGPIO_SetPortBits(E_PT2,i);                  //PT2 Output i=0x0A~0x05
44  }
45
```

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13. GPIO PT1 MANAGEMENT

13.1. Overall description

The PT1 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the input or output IO ports of the capture comparator, SPI, IIC, comparator, PWM and external interrupt modules, etc. Different reuses need different configurations.

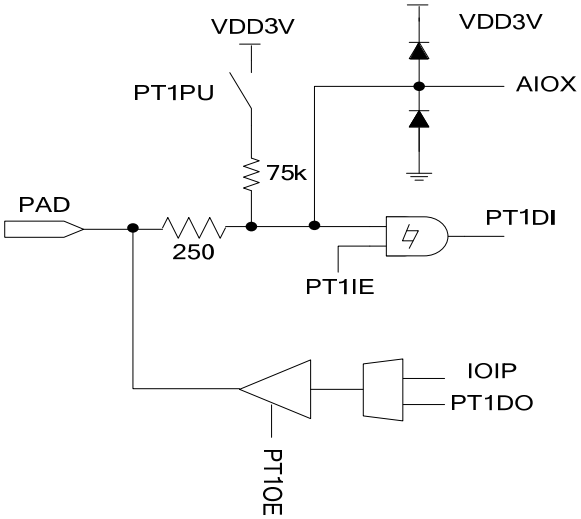

FIG. 13-1 PT1 function block diagram

PT1 has the functions of the input, output, internal pull-up resistors and the external interrupt input port; and different functions should be set by different controllers.

Internal pull-up resistor

The controller PT1PU[7:0] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal 75k pull-up resistor will be enabled; if it is set as <0>, the internal 75k pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.

Output mode

The controller PT1OE[7:0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT1DO[7:0] can

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determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

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Input mode

The controller PT1IE[7:0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. The control bit PT1DI[7:0] can determine whether the input status of the pin of the corresponding IO port is 1 or 0. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

External interrupt input

The PT1 has 8 IO pins, and all of them can be reused as external interrupt input pins. The mode should set the IO port to be the input mode and enable the internal pull-up resistor. It is necessary to set the external interrupt trigger edge by the controller PT1XITT[2:0] and enable the control bit PT1ITD[0] to enable the interrupt trigger edge. The controller PT1XIE[7:0] can enable the interrupt response function of the corresponding IO pin; when the external interrupt signal generates, the interrupt flag of the corresponding IO pin is set as 1. When the global interrupt GIE and the IO external interrupt function are enabled, the chip will stop the current program right away and execute the IO external interrupt program.

13.2. Register address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO base address + 0x00(0x40800)	MASK1	PT1PU	MASK0	PT1OE
GPIO base address + 0x04 (0x40804)	MASK3	PT1IE	MASK2	PT1DO
GPIO base address + 0x08(0x40808)	-	-	-	PT1DI
GPIO base address + 0x0C (0x4080C)	PT1IDF	PT1ITT	PT1ITT	PT1ITT

-Reserved

13.3. Register function

13.3.1. PT1 register PT1CR0

GPIO Base Address + 0x00 (0x40800)									
Symbol	PT1CR0 (PT1 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT1PU7	PT1PU6	PT1PU5	PT1PU4	PT1PU3	PT1PU2	PT1PU1	PT1PU0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT1OE7	PT1OE6	PT1OE5	PT1OE4	PT1OE3	PT1OE2	PT1OE1	PT1OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT1PU	Port 1 internal pull-up control	
		0	Disable the internal pull-up
		1	Enable the internal pull-up
Bit[07~00]	PT1OE	Port 1 PAD output mode enable control	
		0	Disable the output mode
		1	Enable the output mode

13.3.2. PT1 register PT1CR1

GPIO Base Address + 0x04 (0x40804)									
Symbol	PT1CR1 (PT1 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT1IE7	PT1IE6	PT1IE5	PT1IE4	PT1IE3	PT1IE2	PT1IE1	PT1IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT1DO7	PT1DO6	PT1DO5	PT1DO4	PT1DO3	PT1DO2	PT1DO1	PT1DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT1IE	Port 1 PAD input mode control	
		0	Disable the input mode
		1	Enable the input mode
Bit[07~00]	PT1DO	Port 1 PAD output status value	
		0	Output low potential
		1	Output high potential

13.3.3. PT1 register PT1CR2

GPIO Base Address + 0x08 (0x40808)									
Symbol	PT1CR2(PT1 Control Register 2)								
Bit	[31:16]								
Name	-								
RW	-								
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	PT1DI7	PT1DI6	PT1DI5	PT1DI4	PT1DI3	PT1DI2	PT1DI1	PT1DI0
RW	-	R-0							

Bit	Name	Description	
Bit[7~0]	PT1DI	Port1 PAD input status value	
		0	input low potential
		1	input high potential

13.3.4. PT1 register PT1CR3

GPIO Base Address + 0x0C (0x4080C)						
Symbol	PT1CR3 (PT1 Control Register 3)					
Bit	[31:24]	[23:21]	[21:18]	[17:16]		
Name	PT1IDF	PT17ITT	PT16ITT	PT15ITT		
RW	RW-0					
Bit	[15]	[14:12]	[11:9]	[8:6]	[5:3]	[2:0]
Name	PT15ITT	PT14ITT	PT13ITT	PT12ITT	PT11ITT	PT10ITT
RW	RW-0					

Bit	Name	Description	
Bit[31~24]	PT1IDF	PT1 interrupt condition flag when ITT=	
		0	Always 0
		1	Inverse DI
		2	Same as DI
		3	Same as S1
		4	Same as DI
		5	Inverse DI
		6	Same as DI
		7	Inverse DI
Bit[23~00]	PT1#ITT	Port 1.# select the interrupt trigger method	
		000	Disable the GPIO interrupt trigger to not reply to the interrupt.
		001	Rising edge trigger
		010	Falling edge trigger
		011	Potential change trigger

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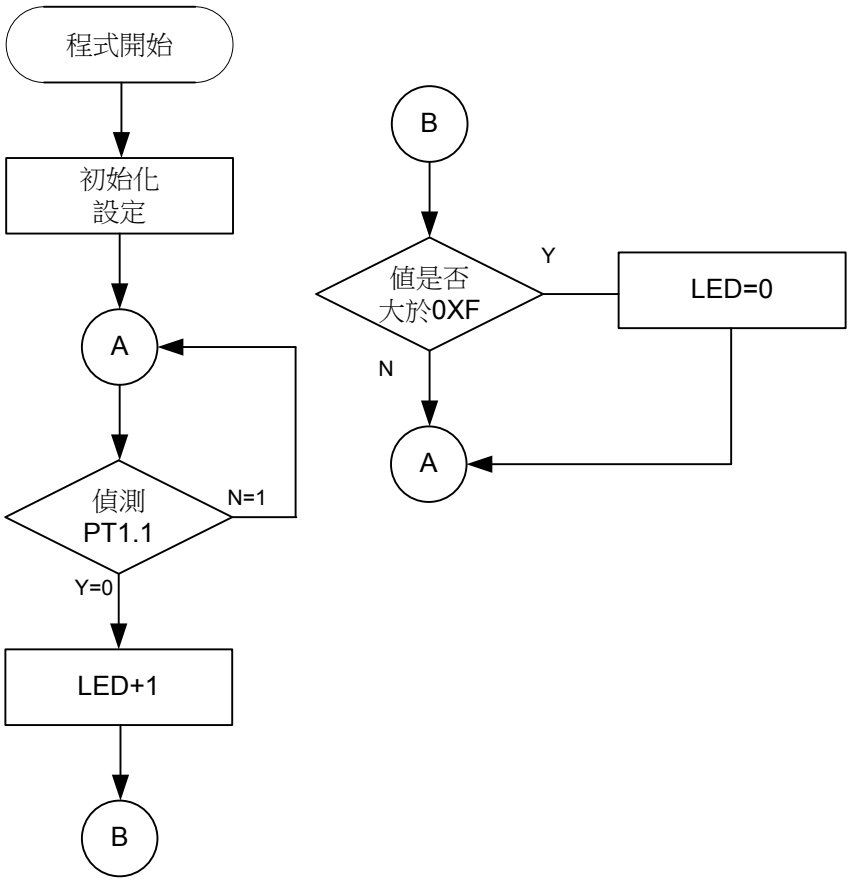
		100	Low potential trigger
		101	High potential trigger
		110	Low potential trigger
		111	High potential trigger

13.4. Model program flow



The program starts
Initialization setting
Detect PT1.1
Is the value higher than 0XF?

13.5. Model program function

Press the PT1.1 for one time will add the LED by 1.
If the LED is added to 0xF, it will be reset to 0. Then, Press the PT1.1 for one time will add the LED by 1.

13.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  void Delay (unsigned int num);
04
05  int main(void)
06  {
07     unsigned int i=0,j=0;
08     DrvGPIO_Open(E_PT1,0x02,E_IO_INPUT);          //Set PT1_1 INPUT
09     DrvGPIO_Open(E_PT1,0x02,E_IO_PullHigh);       //Enable PT1 1 pull hi R
11     DrvGPIO_Open(E_PT2,0x0F,E_IO_OUTPUT);         //Set PT2_0~3 OUTPUT
12
13     while(1)
14     {
15          i=DrvGPIO_GetBit(E_PT1,1);               //Read PT1.1 high or low
16          if(i==0)                                 //IF PT1.1 is low
17          {
18               DrvGPIO_SetPortBits(E_PT2, j++);    //J++
19               if(j>0x0F)j=0x00;                   //IF J>0xF J=0
20          }
21
22     Delay(0x8000);
23  }
24
25  void Delay(unsigned int num)
26  {
27     int a;for(a=0;a<=num;a++);                    //Delay loop
28  }
29
```

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14. GPIO PT2 MANAGEMENT

14.1. Overall description

The PT2 has 8 IO pins, and can be used as common universal IO ports or reused as the input or output IO ports of many function modules, such as capture comparator, SPI, IIC, PWM, external crystal oscillator and external interrupt input, etc. Different reuses need different configurations.

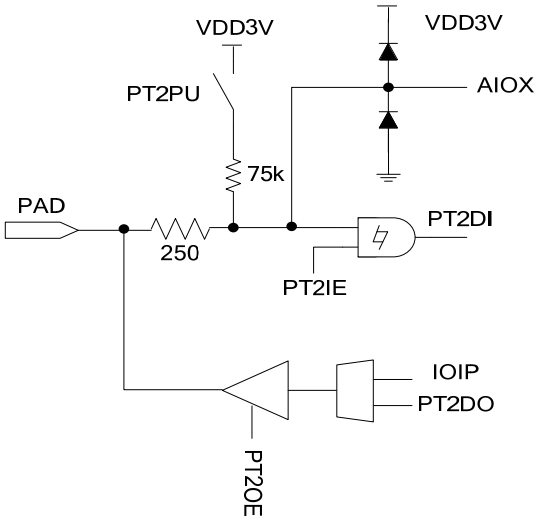

FIG. 14-1 PT2 function block diagram

The PT2 has the functions of the input, output, internal pull-up resistor and external interrupt input port; and different functions need to be set by different controllers.

Internal pull-up resistor

The controller PT2PU[7:0] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal 75k pull-up resistor will be enabled; if the corresponding bit of the IO port is set as <0>, the internal 75k pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.

PS: When PT2.4~PT2.7 serve as the external crystal oscillator input pins, the internal pull-up resistor cannot be enabled, or the crystal oscillator cannot work normally.

Output mode

The controller PT2OE[7:0] can enable or disable the output mode of each IO port, and

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each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT2DO[7:0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0.
Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.
PS: When the PT2.4~PT2.7 serve as the external crystal oscillator input pins, the output mode should be disabled.

Input mode

The controller PT2IE[7:0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT2DI[7:0]. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

External interrupt input

The PT2 has 8 IO pins, and all of them can be reused as external interrupt input pins. The mode should set the IO port to be the input mode and enable the internal pull-up resistor. It is necessary to set the external interrupt trigger edge by the controller PT2XITT[2:0] and enable the control bit PT2ITD[0] to enable the interrupt trigger edge. The controller PT2XIE[7:0] can enable the interrupt response function of the corresponding IO pin; when the external interrupt signal generates, the interrupt flag of the corresponding IO pin is set as 1. When the global interrupt GIE and the IO external interrupt function are enabled, the chip will stop the current program right away and execute the IO external interrupt program.

14.2. Register address

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GPIO Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x10(0x40810)	MASK1		PT2PU		MASK0		PT2OE	
GPIO Base Address + 0x14 (0x40814)	MASK3		PT2IE		MASK2		PT2DO	
GPIO Base Address + 0x18(0x40818)	-		-		-		PT2DI	
GPIO Base Address + 0x1C (0x4081C)	PT2IDF		PT2ITT		PT2ITT		PT2ITT	

-Reserved

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14.3. Register function

14.3.1. PT2 register PT2CR0

GPIO Base Address + 0x10 (0x40810)									
Symbol	PT2CR0 (PT2 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT2PU7	PT2PU6	PT2PU5	PT2PU4	PT2PU3	PT2PU2	PT2PU1	PT2PU0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT2OE7	PT2OE6	PT2OE5	PT2OE4	PT2OE3	PT2OE2	PT2OE1	PT2OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT2PU	Port 2 internal pull-up control	
		0	Disable the internal pull-up
		1	Enable the internal pull-up
Bit[07~00]	PT2OE	Port 2 PAD output mode enable control	
		0	Disable the output mode
		1	Enable the output mode

14.3.2. 1PT2 register PT2CR1

GPIO Base Address + 0x14 (0x40814)									
Symbol	PT2CR1 (PT2 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT2IE7	PT2IE6	PT2IE5	PT2IE4	PT2IE3	PT2IE2	PT2IE1	PT2IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT2DO7	PT2DO6	PT2DO5	PT2DO4	PT2DO3	PT2DO2	PT2DO1	PT2DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT2IE	Port 2 PAD input mode enable control	
		0	Disable the input mode
		1	Enable the input mode
Bit[7~0]	PT2DO	Port 2 PAD output status value	
		0	Output low potential
		1	Output high potential

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14.3.3. PT2 register PT2CR2

GPIO Base Address + 0x18 (0x40818)									
Symbol	PT2CR2 (PT2 Control Register 2)								
Bit	[31:16]								
Name	-								
RW	-								
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	PT2DI[7]	PT2DI[6]	PT2DI[5]	PT2DI[4]	PT2DI[3]	PT2DI[2]	PT2DI[1]	PT2DI[0]
RW	-	R-0							

Bit	Name	Description	
Bit[7~0]	PT2DI	Port2 PAD input status value	
		0	Input low potential
		1	Input high potential

14.3.4. PT2 register PT2CR3

GPIO Base Address + 0x1C (0x4081C)						
Symbol	PT2CR3 (PT2 Control Register 3)					
Bit	[31:24]		[23:21]	[21:18]	[17:16]	
Name	PT2IDF		PT27ITT	PT26ITT	PT25ITT	
RW	RW-0					
Bit	[15]	[14:12]	[11:9]	[8:6]	[5:3]	[2:0]
Name	PT25ITT	PT24ITT	PT23ITT	PT22ITT	PT21ITT	PT20ITT
RW	RW-0					

Bit	Name	Description	
Bit[31~24]	PT2IDF	PT2 interrupt condition flag When ITT=	
		0	Always 0
		1	Inverse DI
		2	Same as DI
		3	Same as S1
		4	Same as DI
		5	Inverse DI
		6	Same as DI
		7	Inverse DI
Bit[23~00]	PT2#ITT	Port 2.# select the interrupt trigger method	
		000	Disable the GPIO interrupt trigger to not reply to the interrupt.
		001	Rising edge trigger
		010	Falling edge trigger

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		011	Potential change trigger
		100	Low potential trigger
		101	High potential trigger
		110	Low potential trigger
		111	High potential trigger

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15. GPIO PT3 MANAGEMENT

15.1. Overall description

The PT3 has 8 IO pins, and can be used as common universal IO ports or reused as the input or output IO ports of many function modules, such as OP amplifier, DAC and ADC converters, etc. Different reuses need different configurations.

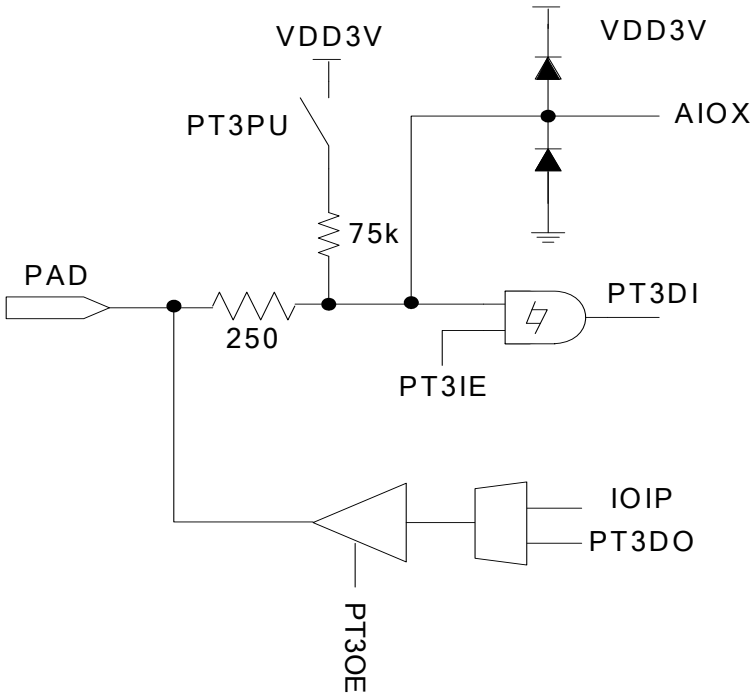

FIG. 15-1 PT3 function block diagram

The PT3 has the functions of the input, output and internal pull-up resistors; and different functions need to be set by different controllers.

Internal pull-up resistor

The controller PT3PU[7:0] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal 75k pull-up resistor will be enabled; if it is set as <0>, the internal 75k pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.

Output mode

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The controller PT3OE[7:0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT3DO[7:0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT3IE[7:0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input status of the corresponding IO pin is 1 or 0 can be read via the controller PT3DI[7:0]. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

15.2. Register address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO Base Address + 0x20(0x40820)	MASK1	PT3PU	MASK0	PT3OE
GPIO Base Address + 0x24 (0x40824)	MASK3	PT3IE	MASK2	PT3DO
GPIO Base Address + 0x28(0x40828)	-	-	REG4	PT3DI

-Reserved

15.3. Register function

15.3.1. PT3 register PT3CR0

GPIO Base Address + 0x20 (0x40820)									
Symbol	PT3CR0 (PT3 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT3PU7	PT3PU6	PT3PU5	PT3PU4	PT3PU3	PT3PU2	PT3PU1	PT3PU0

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RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT3OE7	PT3OE6	PT3OE5	PT3OE4	PT3OE3	PT3OE2	PT3OE1	PT3OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT3PU	Port 3 internal pull-up enable control	
		0	Disable the internal pull-up
		1	Enable the internal pull-up
Bit[7~0]	PT3OE	Port 3 PAD output mode enable control	
		0	Disable the output mode
		1	Enable the output mode

15.3.2. PT3 register PT3CR1

GPIO Base Address + 0x24 (0x40824)									
Symbol	PT3CR1 (PT3 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT3IE7	PT3IE6	PT3IE5	PT3IE4	PT3IE3	PT3IE2	PT3IE1	PT3IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT3DO7	PT3DO6	PT3DO5	PT3DO4	PT3DO3	PT3DO2	PT3DO1	PT3DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT3IE	Port 3 PAD input mode enable control	
		0	Disable the input mode
		1	Enable the input mode
Bit[7~0]	PT3DO	Port 3 PAD output status value	
		0	Output low potential
		1	Output high potential

15.3.3. PT3 register PT3CR2

GPIO Base Address + 0x28 (0x40828)									
Symbol	PT3CR2 (PT3 Control Register 2)								
Bit	[31:24]	[23:18]						[17]	[16]
Name	MASK	-						PT3AO	-
RW	R0W-0	-						R-X	-
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]

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Name	-	PT3DI[7]	PT3DI[6]	PT3DI[5]	PT3DI[4]	PT3DI[3]	PT3DI[2]	PT3DI[1]	PT3DI[0]
RW	-	R-0							

Bit	Name	Description	
Bit[17]	PT3A0	DAO outputs to the PT3.1 enable control	
		0	Disable
		1	Enable
Bit[7~0]	PT3DI	Port3 PAD input status value	
		0	input low potential
		1	input high potential

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16. GPIO PT6 MANAGEMENT

16.1. Overall description

The PT6 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the LCD function output port. Different reuses need different configurations.

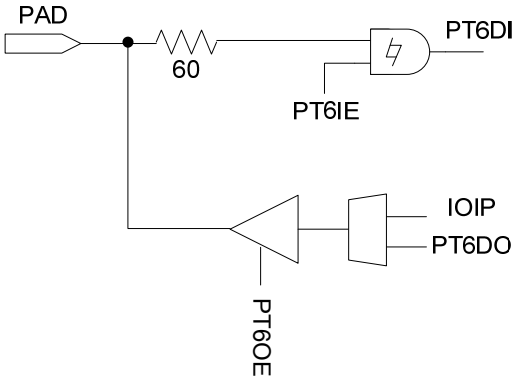

FIG. 16-1 PT6 function block diagram

The PT6 has input and output functions; and different functions should be set by different controllers.

Output mode

The controller PT6xOE[0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT6xDO[0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT6xIE[0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT6xDI[0]. If the IO is set as the input mode and the chip should be connected to the external pull-up resistor; and

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the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

LCD mode

The controller SEGx[5:0] determines the output data of the LCD SEGMENT. If the LCD is under the 1/6 duty mode, the SEGx[5:0] can determine the data content of the 1/6 duty data content; if the LCD is under the 1/5 duty mode, the SEGx[4:0] can determine the 1/5 duty data content; if the LCD is under the 1/4 duty mode, the SEGx[3:0] can determine the 1/4 duty data content; if the LCD is under the 1/3 duty mode, the SEGx[2:0] can determine the 1/3 duty data content.

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16.2. Register address

GPIO Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x50(0x40850)	MASK1		PT61CFG		MASK0		PT60CFG	
GPIO Base Address + 0x54(0x40854)	MASK3		PT63CFG		MASK2		PT62CFG	
GPIO Base Address + 0x58(0x40858)	MASK5		PT65CFG		MASK4		PT64CFG	
GPIO Base Address + 0x5C(0x4085C)	MASK7		PT67CFG		MASK6		PT66CFG	

LCD Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x50(0x40850)	MASK1		SEG3		MASK0		SEG2	
GPIO Base Address + 0x54(0x40854)	MASK3		SEG5		MASK2		SEG4	
GPIO Base Address + 0x58(0x40858)	MASK5		SEG7		MASK4		SEG6	
GPIO Base Address + 0x5C(0x4085C)	MASK7		SEG9		MASK6		SEG8	

LCD Register Address 0x41B04 can determine the setting is the GPIO Mode or the LCD Mode.

16.3. Register function

16.3.1. PT6.0/PT6.1 register

When GPIO Mode.

GPIO Base Address + 0x50 (0x40850)									
Symbol	PT60CFG/ PT61CFG (PT6 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT61OE	PT61IE	PT61DO	PT61DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT60OE	PT60IE	PT60DO	PT60DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT61OE	PT6.1 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT61IE	PT6.1 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT61DO	PT6.1 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT61DI	PT6.1 Input Data	
		0	Input Low

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		1	Input High
Bit[3]	PT60OE	PT6.0 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT60IE	PT6.0 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT60DO	PT6.0 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT60DI	PT6.0 Input Data	
		0	Input Low
		1	Input High

When LCD Mode

GPIO Base Address + 0x50 (0x40850)									
Symbol	SEG2/SEG3 (PT6 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG3 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG2 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 3 Data	LCD Segment 3 Data
		Segment Data
Bit[5~0]	SEG 2 Data	LCD Segment 2 Data
		Segment Data

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16.3.2. PT6.2/PT6.3 register

When GPIO Mode.

GPIO Base Address + 0x54 (0x40854)									
Symbol	PT62CFG/ PT63CFG (PT6 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT63OE	PT63IE	PT63DO	PT63DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT62OE	PT62IE	PT62DO	PT62DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT63OE	PT6.3 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT63IE	PT6.3 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT63DO	PT6.3 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT63DI	PT6.3 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT62OE	PT6.2 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT62IE	PT6.2 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT62DO	PT6.2 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT62DI	PT6.2 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x54 (0x40854)									
Symbol	SEG4/SEG5 (PT6 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG5 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG4 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 5 Data	LCD Segment 5 Data
		Segment Data
Bit[5~0]	SEG 4 Data	LCD Segment 4 Data
		Segment Data

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16.3.3. PT6.4/PT6.5 register

When GPIO Mode.

GPIO Base Address + 0x58 (0x40858)									
Symbol	PT64CFG/ PT65CFG (PT6 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT65OE	PT65IE	PT65DO	PT65DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT64OE	PT64IE	PT64DO	PT64DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT65OE	PT6.5 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT65IE	PT6.5 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT65DO	PT6.5 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT65DI	PT6.5 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT64OE	PT6.4 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT64IE	PT6.4 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT64DO	PT6.4 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT64DI	PT6.4 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x58 (0x40858)									
Symbol	SEG6/SEG7 (PT6 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG7 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG6 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 7 Data	LCD Segment 7 Data
		Segment Data
Bit[5~0]	SEG 6 Data	LCD Segment 6 Data
		Segment Data

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16.3.4. PT6.6/PT6.7 register

When GPIO Mode.

GPIO Base Address + 0x5C (0x4085C)									
Symbol	PT66CFG/ PT67CFG (PT6 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT67OE	PT67IE	PT67DO	PT67DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT66OE	PT66IE	PT66DO	PT66DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT67OE	PT6.7 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT67IE	PT6.7 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT67DO	PT6.7 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT67DI	PT6.7 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT66OE	PT6.6 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT66IE	PT6.6 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT66DO	PT6.6 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT66DI	PT6.6 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x5C (0x4085C)									
Symbol	SEG8/SEG9 (PT6 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG9 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG8 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 9 Data	LCD Segment 9 Data
		Segment Data
Bit[5~0]	SEG 8 Data	LCD Segment 8 Data
		Segment Data

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17. GPIO PT7 MANAGEMENT

17.1. Overall description

The PT7 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the LCD function output port. Different reuses need different configurations.

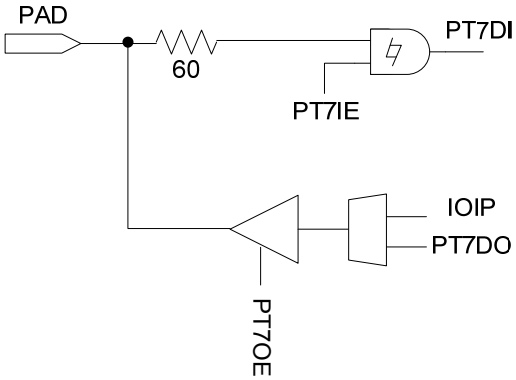

FIG. 17-1 PT7 function block diagram

The PT7 has input and output functions; and different functions should be set by different controllers.

Output mode

The controller PT7xOE[0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT7xDO[0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT7xIE[0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT7xDI[0]. If the IO is set as the input mode and the chip should be connected to the external pull-up resistor; and

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the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

LCD mode

The controller SEGx[5:0] determines the output data of the LCD SEGMENT. If the LCD is under the 1/6 duty mode, the SEGx[5:0] can determine the data content of the 1/6 duty data content; if the LCD is under the 1/5 duty mode, the SEGx[4:0] can determine the 1/5 duty data content; if the LCD is under the 1/4 duty mode, the SEGx[3:0] can determine the 1/4 duty data content; if the LCD is under the 1/3 duty mode, the SEGx[2:0] can determine the 1/3 duty data content.

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17.2. Register address

GPIO Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x60(0x40860)	MASK1		PT71CFG		MASK0		PT70CFG	
GPIO Base Address + 0x64(0x40864)	MASK3		PT73CFG		MASK2		PT72CFG	
GPIO Base Address + 0x68(0x40868)	MASK5		PT75CFG		MASK4		PT74CFG	
GPIO Base Address + 0x6C(0x4086C)	MASK7		PT77CFG		MASK6		PT76CFG	

LCD Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x60(0x40860)	MASK1		SEG11		MASK0		SEG10	
GPIO Base Address + 0x64(0x40864)	MASK3		SEG13		MASK2		SEG12	
GPIO Base Address + 0x68(0x40868)	MASK5		SEG15		MASK4		SEG14	
GPIO Base Address + 0x6C(0x4086C)	MASK7		SEG17		MASK6		SEG16	

LCD Register Address 0x41B04 can determine the setting is the GPIO Mode or the LCD Mode.

17.3. Register function

17.3.1. PT7.0/PT7.1 register

When GPIO Mode.

GPIO Base Address + 0x60 (0x40860)									
Symbol	PT70CFG/ PT71CFG (PT7 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT71OE	PT71IE	PT71DO	PT71DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT70OE	PT70IE	PT70DO	PT70DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT71OE	PT7.1 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT71IE	PT7.1 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT71DO	PT7.1 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT71DI	PT7.1 Input Data	
		0	Input Low

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		1	Input High
Bit[3]	PT70OE	PT7.0 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT70IE	PT7.0 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT70DO	PT7.0 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT70DI	PT7.0 Input Data	
		0	Input Low
		1	Input High

When LCD Mode

GPIO Base Address + 0x60 (0x40860)									
Symbol	SEG10/SEG11 (PT7 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG11 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG10 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 11 Data	LCD Segment 11 Data
		Segment Data
Bit[5~0]	SEG 10 Data	LCD Segment 10 Data
		Segment Data

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17.3.2. PT7.2/PT7.3 register

When GPIO Mode.

GPIO Base Address + 0x64 (0x40864)									
Symbol	PT72CFG/ PT73CFG (PT7 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT73OE	PT73IE	PT73DO	PT73DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT72OE	PT72IE	PT72DO	PT72DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT73OE	PT7.3 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT73IE	PT7.3 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT73DO	PT7.3 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT73DI	PT7.3 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT72OE	PT7.2 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT72IE	PT7.2 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT72DO	PT7.2 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT72DI	PT7.2 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x64 (0x40864)									
Symbol	SEG12/SEG13 (PT7 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG13 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG12 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 13 Data	LCD Segment 13 Data
		Segment Data
Bit[5~0]	SEG 12 Data	LCD Segment 12 Data
		Segment Data

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17.3.3. PT7.4/PT7.5 register

When GPIO Mode.

GPIO Base Address + 0x68 (0x40868)									
Symbol	PT74CFG/ PT75CFG (PT7 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT75OE	PT75IE	PT75DO	PT75DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT74OE	PT74IE	PT74DO	PT74DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT75OE	PT7.5 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT75IE	PT7.5 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT75DO	PT7.5 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT75DI	PT7.5 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT74OE	PT7.4 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT74IE	PT7.4 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT74DO	PT7.4 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT74DI	PT7.4 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x68 (0x40868)									
Symbol	SEG14/SEG15 (PT7 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG15 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG14 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 15 Data	LCD Segment 15 Data
		Segment Data
Bit[5~0]	SEG 14 Data	LCD Segment 14 Data
		Segment Data

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17.3.4. PT7.6/PT7.7 register

When GPIO Mode.

GPIO Base Address + 0x6C (0x4086C)									
Symbol	PT76CFG/ PT77CFG (PT7 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT77OE	PT77IE	PT77DO	PT77DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT76OE	PT76IE	PT76DO	PT76DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT77OE	PT7.7 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT77IE	PT7.7 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT77DO	PT7.7 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT77DI	PT7.7 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT76OE	PT7.6 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT76IE	PT7.6 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT76DO	PT7.6 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT76DI	PT7.6 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x6C (0x4086C)									
Symbol	SEG16/SEG17 (PT7 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG17 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG16 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 17 Data	LCD Segment 17 Data
		Segment Data
Bit[5~0]	SEG 16 Data	LCD Segment 16 Data
		Segment Data

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18. GPIO PT8 MANAGEMENT

18.1. Overall description

The PT8 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the LCD function output port. Different reuses need different configurations.

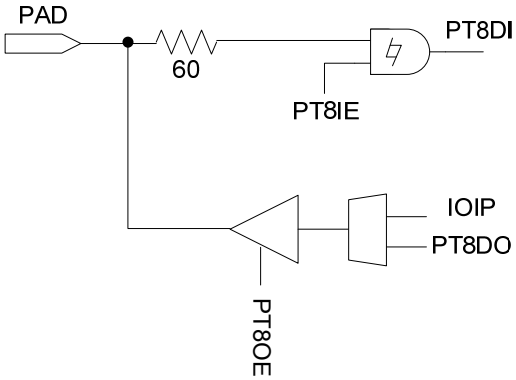

FIG. 18-1 PT8 function block diagram

The PT8 has input and output functions; and different functions should be set by different controllers.

Output mode

The controller PT8xOE[0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT8xDO[0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT8xIE[0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT8xDI[0]. If the IO is set as the input mode and the chip should be connected to the external pull-up resistor; and

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the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

LCD mode

The controller SEGx[5:0] determines the output data of the LCD SEGMENT. If the LCD is under the 1/6 duty mode, the SEGx[5:0] can determine the data content of the 1/6 duty data content; if the LCD is under the 1/5 duty mode, the SEGx[4:0] can determine the 1/5 duty data content; if the LCD is under the 1/4 duty mode, the SEGx[3:0] can determine the 1/4 duty data content; if the LCD is under the 1/3 duty mode, the SEGx[2:0] can determine the 1/3 duty data content.

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18.2. Register address

GPIO Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x70(0x40870)	MASK1		PT81CFG		MASK0		PT80CFG	
GPIO Base Address + 0x74(0x40874)	MASK3		PT83CFG		MASK2		PT82CFG	
GPIO Base Address + 0x78(0x40878)	MASK5		PT85CFG		MASK4		PT84CFG	
GPIO Base Address + 0x7C(0x4087C)	MASK7		PT87CFG		MASK6		PT86CFG	

LCD Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x70(0x40870)	MASK1		SEG19		MASK0		SEG18	
GPIO Base Address + 0x74(0x40874)	MASK3		SEG21		MASK2		SEG20	
GPIO Base Address + 0x78(0x40878)	MASK5		SEG23		MASK4		SEG22	
GPIO Base Address + 0x7C(0x4087C)	MASK7		SEG25		MASK6		SEG24	

LCD Register Address 0x41B04 can determine the setting is the GPIO Mode or the LCD Mode.

18.3. Register function

18.3.1. PT8.0/PT8.1 register

When GPIO Mode.

GPIO Base Address + 0x70 (0x40870)									
Symbol	PT80CFG/ PT81CFG (PT8 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT81OE	PT81IE	PT81DO	PT81DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT80OE	PT80IE	PT80DO	PT80DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT81OE	PT8.1 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT81IE	PT8.1 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT81DO	PT8.1 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT81DI	PT8.1 Input Data	
		0	Input Low

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		1	Input High
Bit[3]	PT80OE	PT8.0 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT80IE	PT8.0 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT80DO	PT8.0 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT80DI	PT8.0 Input Data	
		0	Input Low
		1	Input High

When LCD Mode

GPIO Base Address + 0x70 (0x40870)									
Symbol	SEG18/SEG19 (PT8 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG19 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG18 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 19 Data	LCD Segment 19 Data
		Segment Data
Bit[5~0]	SEG 18 Data	LCD Segment 18 Data
		Segment Data

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18.3.2. PT8.2/PT8.3 register

When GPIO Mode.

GPIO Base Address + 0x74 (0x40874)									
Symbol	PT82CFG/ PT83CFG (PT8 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT83OE	PT83IE	PT83DO	PT83DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT82OE	PT82IE	PT82DO	PT82DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT83OE	PT8.3 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT83IE	PT8.3 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT83DO	PT8.3 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT83DI	PT8.3 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT82OE	PT8.2 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT82IE	PT8.2 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT82DO	PT8.2 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT82DI	PT8.2 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x74 (0x40874)									
Symbol	SEG20/SEG21 (PT8 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG21 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG20 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 21 Data	LCD Segment 21 Data
		Segment Data
Bit[5~0]	SEG 20 Data	LCD Segment 20 Data
		Segment Data

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18.3.3. PT8.4/PT8.5 register

When GPIO Mode.

GPIO Base Address + 0x78 (0x40878)									
Symbol	PT84CFG/ PT85CFG (PT8 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT85OE	PT85IE	PT85DO	PT85DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT84OE	PT84IE	PT84DO	PT84DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT85OE	PT8.5 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT85IE	PT8.5 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT85DO	PT8.5 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT85DI	PT8.5 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT84OE	PT8.4 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT84IE	PT8.4 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT84DO	PT8.4 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT84DI	PT8.4 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x78 (0x40878)									
Symbol	SEG22/SEG23 (PT8 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG23 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG22 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 23 Data	LCD Segment 23 Data
		Segment Data
Bit[5~0]	SEG 22 Data	LCD Segment 22 Data
		Segment Data

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18.3.4. PT8.6/PT8.7 register

When GPIO Mode.

GPIO Base Address + 0x7C (0x4087C)									
Symbol	PT86CFG/ PT87CFG (PT8 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT87OE	PT87IE	PT87DO	PT87DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT86OE	PT86IE	PT86DO	PT86DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT87OE	PT8.7 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT87IE	PT8.7 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT87DO	PT8.7 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT87DI	PT8.7 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT86OE	PT8.6 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT86IE	PT8.6 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT86DO	PT8.6 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT86DI	PT8.6 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x7C (0x4087C)									
Symbol	SEG24/SEG25 (PT8 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG25 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG24 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 25 Data	LCD Segment 25 Data
		Segment Data
Bit[5~0]	SEG 24 Data	LCD Segment 24 Data
		Segment Data

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19. GPIO PT9 MANAGEMENT

19.1. Overall description

The PT9 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the LCD function output port. Different reuses need different configurations.

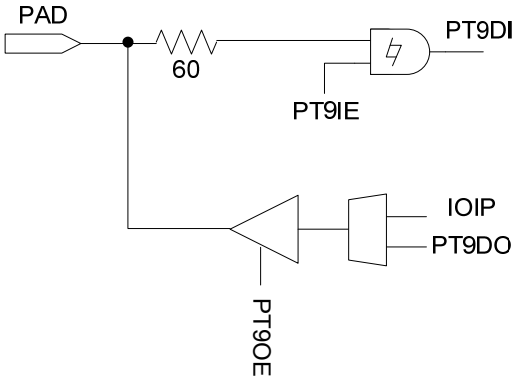

FIG. 19-1 PT9 function block diagram

The PT9 has input and output functions; and different functions should be set by different controllers.

Output mode

The controller PT9xOE[0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT9xDO[0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT9xIE[0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT9xDI[0]. If the IO is set as the input mode and the chip should be connected to the external pull-up resistor; and the

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IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

LCD mode

The controller SEGx[5:0] determines the output data of the LCD SEGMENT. If the LCD is under the 1/6 duty mode, the SEGx[5:0] can determine the data content of the 1/6 duty data content; if the LCD is under the 1/5 duty mode, the SEGx[4:0] can determine the 1/5 duty data content; if the LCD is under the 1/4 duty mode, the SEGx[3:0] can determine the 1/4 duty data content; if the LCD is under the 1/3 duty mode, the SEGx[2:0] can determine the 1/3 duty data content.

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19.2. Register address

GPIO Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x80(0x40880)	MASK1		PT91CFG		MASK0		PT90CFG	
GPIO Base Address + 0x84(0x40884)	MASK3		PT93CFG		MASK2		PT92CFG	
GPIO Base Address + 0x88(0x40888)	MASK5		PT95CFG		MASK4		PT94CFG	
GPIO Base Address + 0x8C(0x4088C)	MASK7		PT97CFG		MASK6		PT96CFG	

LCD Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x80(0x40880)	MASK1		SEG27		MASK0		SEG26	
GPIO Base Address + 0x84(0x40884)	MASK3		SEG29		MASK2		SEG28	
GPIO Base Address + 0x88(0x40888)	MASK5		SEG31		MASK4		SEG30	
GPIO Base Address + 0x8C(0x4088C)	MASK7		SEG33		MASK6		SEG32	

LCD Register Address 0x41B04 can determine the setting is the GPIO Mode or the LCD Mode.

19.3. Register function

19.3.1. PT9.0/PT9.1 register

When GPIO Mode.

GPIO Base Address + 0x80 (0x40880)									
Symbol	PT90CFG/ PT91CFG (PT9 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT91OE	PT91IE	PT91DO	PT91DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT90OE	PT90IE	PT90DO	PT90DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT91OE	PT9.1 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT91IE	PT9.1 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT91DO	PT9.1 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT91DI	PT9.1 Input Data	
		0	Input Low

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		1	Input High
Bit[3]	PT90OE	PT9.0 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT90IE	PT9.0 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT90DO	PT9.0 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT90DI	PT9.0 Input Data	
		0	Input Low
		1	Input High

When LCD Mode

GPIO Base Address + 0x80 (0x40880)									
Symbol	SEG26/SEG27 (PT9 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG27 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG26 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 27 Data	LCD Segment 27 Data
		Segment Data
Bit[5~0]	SEG 26 Data	LCD Segment 26 Data
		Segment Data

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19.3.2. PT9.2/PT9.3 register

When GPIO Mode.

GPIO Base Address + 0x84 (0x40884)									
Symbol	PT92CFG/ PT93CFG (PT9 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT93OE	PT93IE	PT93DO	PT93DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT92OE	PT92IE	PT92DO	PT92DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT93OE	PT9.3 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT93IE	PT9.3 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT93DO	PT9.3 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT93DI	PT9.3 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT92OE	PT9.2 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT92IE	PT9.2 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT92DO	PT9.2 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT92DI	PT9.2 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x84 (0x40884)									
Symbol	SEG28/SEG29 (PT9 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG29 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG28 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 29 Data	LCD Segment 29 Data
		Segment Data
Bit[5~0]	SEG 28 Data	LCD Segment 28 Data
		Segment Data

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19.3.3. PT9.4/PT9.5 register

When GPIO Mode.

GPIO Base Address + 0x88 (0x40888)									
Symbol	PT94CFG/ PT95CFG (PT9 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT95OE	PT95IE	PT95DO	PT95DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT94OE	PT94IE	PT94DO	PT94DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT95OE	PT9.5 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT95IE	PT9.5 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT95DO	PT9.5 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT95DI	PT9.5 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT94OE	PT9.4 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT94IE	PT9.4 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT94DO	PT9.4 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT94DI	PT9.4 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x88 (0x40888)									
Symbol	SEG30/SEG31 (PT9 Control Register 2)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG31 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG30 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 31 Data	LCD Segment 31 Data
		Segment Data
Bit[5~0]	SEG 30 Data	LCD Segment 30 Data
		Segment Data

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19.3.4. PT9.6/PT9.7 register

When GPIO Mode.

GPIO Base Address + 0x8C (0x4088C)									
Symbol	PT96CFG/ PT97CFG (PT9 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT97OE	PT97IE	PT97DO	PT97DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT96OE	PT96IE	PT96DO	PT96DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT97OE	PT9.7 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT97IE	PT9.7 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT97DO	PT9.7 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT97DI	PT9.7 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT96OE	PT9.6 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT96IE	PT9.6 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT96DO	PT9.6 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT96DI	PT9.6 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x8C (0x4088C)									
Symbol	SEG32/SEG33 (PT9 Control Register 3)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG33 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG32 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 33 Data	LCD Segment 33 Data
		Segment Data
Bit[5~0]	SEG 32 Data	LCD Segment 32 Data
		Segment Data

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20. GPIO PT10 MANAGEMENT

20.1. Overall description

The PT10 has 4 IO pins, which can be used as the common universal IO ports, and can also be reused as the LCD function output port. Different reuses need different configurations.

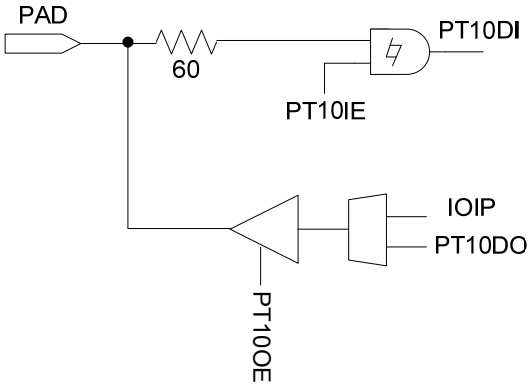

FIG. 20-1 PT10 function block diagram

The PT10 has input and output functions; and different functions should be set by different controllers.

Output mode

The controller PT10xOE[0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT10xDO[0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT10xIE[0] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT10xDI[0]. If the IO is set as the input mode and the chip should be connected to the external pull-up resistor; and the IO pin is not allowed to be floating in order to prevent from the electric leakage of the

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chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

LCD mode

The controller SEGx[5:0] determines the output data of the LCD SEGMENT. If the LCD is under the 1/6 duty mode, the SEGx[5:0] can determine the data content of the 1/6 duty data content; if the LCD is under the 1/5 duty mode, the SEGx[4:0] can determine the 1/5 duty data content; if the LCD is under the 1/4 duty mode, the SEGx[3:0] can determine the 1/4 duty data content; if the LCD is under the 1/3 duty mode, the SEGx[2:0] can determine the 1/3 duty data content; but the SEG0 only supports the 1/3 duty and 1/4duty; and the SEG1 supports the 1/3 duty, 1/4 duty and 1/5duty.

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20.2. Register address

GPIO Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x90(0x40890)	MASK1		PT101CFG		MASK0		PT100CFG	
GPIO Base Address + 0x94(0x40894)	MASK3		PT103CFG		MASK2		PT102CFG	

LCD Mode Register Address	31	24	23	16	15	8	7	0
GPIO Base Address + 0x90(0x40890)	MASK1		SEG35		MASK0		SEG34	
GPIO Base Address + 0x94(0x40894)	MASK3		SEG1		MASK2		SEG0	

LCD Register Address 0x41B04 can determine the setting is the GPIO Mode or the LCD Mode.

20.3. Register function

20.3.1. PT10.0/PT10.1 register

When GPIO Mode.

GPIO Base Address + 0x90 (0x40890)									
Symbol	PT100CFG/ PT101CFG (PT10 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT101OE	PT101IE	PT101DO	PT101DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT100OE	PT100IE	PT100DO	PT100DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT101OE	PT10.1 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT101IE	PT10.1 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT101DO	PT10.1 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT101DI	PT10.1 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT100OE	PT10.0 Output Enable	
		0	Disable

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		1	Enable
Bit[2]	PT100IE	PT10.0 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT100DO	PT10.0 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT100DI	PT10.0 Input Data	
		0	Input Low
		1	Input High

When LCD Mode

GPIO Base Address + 0x90 (0x40890)									
Symbol	SEG34/SEG35 (PT10 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	SEG35 Data					
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	SEG34 Data					
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[21~16]	SEG 35 Data	LCD Segment 35 Data
		Segment Data
Bit[5~0]	SEG 34 Data	LCD Segment 34 Data
		Segment Data

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20.3.2. PT10.2/PT10.3 register

When GPIO Mode.

GPIO Base Address + 0x94 (0x40894)									
Symbol	PT102CFG/ PT103CFG (PT10 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	-	PT103OE	PT103IE	PT103DO	PT103DI
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	-	-	PT102OE	PT102IE	PT102DO	PT102DI
RW	R0W-0	RW-0							RW-1

Bit	Name	Description	
Bit[19]	PT103OE	PT10.3 Output Enable	
		0	Disable
		1	Enable
Bit[18]	PT103IE	PT10.3 Input Enable	
		0	Disable
		1	Enable
Bit[17]	PT103DO	PT10.3 Output Data	
		0	Output Low
		1	Output High
Bit[16]	PT103DI	PT10.3 Input Data	
		0	Input Low
		1	Input High
Bit[3]	PT102OE	PT10.2 Output Enable	
		0	Disable
		1	Enable
Bit[2]	PT102IE	PT10.2 Input Enable	
		0	Disable
		1	Enable
Bit[1]	PT102DO	PT10.2 Output Data	
		0	Output Low
		1	Output High
Bit[0]	PT102DI	PT10.2 Input Data	
		0	Input Low
		1	Input High

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When LCD Mode

GPIO Base Address + 0x94 (0x40894)									
Symbol	SEG0/SEG1 (PT10 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-		SEG1 Data				
RW	R0W-0	RW-0							RW-1
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-			SEG0 Data			
RW	R0W-0	RW-0							RW-1

Bit	Name	Description
Bit[20~16]	SEG 1 Data	LCD Segment 1 Data (support 1/3 or 1/4 or 1/5 duty mode)
		Segment Data
Bit[3~0]	SEG 0 Data	LCD Segment 0 Data (support 1/3 or 1/4 duty mode)
		Segment Data

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21. GPIO MANAGEMENT

21.1. Overall description

The chip has multiple universal IO ports, and most of them have reuse functions; their reuse functions should be controlled by the registers. The chapter will introduce the control of the reuse functions of the IO ports.

Each IO port has multiple reuse functions but only one of these functions can work at a time; thus, if it is not necessary to use the reuse functions, please remember to disable them for other functions. However, some reuse functions can work together, such as PT1/PT2; when they are set as the external input ports, they can be set as the input ports of the IIC, SPI and UART, etc. Please note that the above situation is on the condition that they are set as the input ports; in this way, the external interrupt functions generated by communication can be realized by the communication signals and the external interrupt functions.

In general, the reuse functions should be used on a group basis and only one group can work at a time. If the SPI function is used, the CS_1, CK_1, MISO_1 and MOSI_1 are the first group, and the CS_2, CK_2, MISO_2 and MOSI_2 are the second group, and so on. When using the SPI, the user can select the first group or the second group according to the actual requirements but only one group can work at a time. When the user needs use the communication SPI, I2C, UART and the like, the user can set the SPI to use the first group (CS_1, CK_1, MISO_1 and MOSI_1), set the I2C to use the third group (SCL_3 and SDA_3), and set the UART to use the third group (Tx_3 and Rx_3). In this way, the desired effect can be achieved by the different configuration of the pins.

The following table lists the reuse functions of all IO pins and their priority level; 0 stands for the highest level and 6 stands for the lowest level.

Function	INT	Timer C Capture	Special Function	SPI	I2C	UART	Analog IP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT1.0	INT1.0	TCI1_1		CS_1	SCL_1	Tx_1		CH1	PWM0_1
PT1.1	INT1.1	TCI2_1		CK_1	SDA_1	Rx_1		CH2	PWM1_1
PT1.2	INT1.2	TCI1_2		MISO_1	SCL_2	Tx2_1		CH3	PWM2_1
PT1.3	INT1.3	TCI2_2		MOSI_1	SDA_2	Rx2_1		CL1	PWM3_1
PT1.4	INT1.4	TCI1_3		CS_2	SCL_3	Tx_2		CL2	PWM0_2
PT1.5	INT1.5	TCI2_3		CK_2	SDA_3	Rx_2		CL3	PWM1_2
PT1.6	INT1.6	TCI1_4		MISO_2	SCL_4	Tx2_2		CL4	PWM2_2
PT1.7	INT1.7	TCI2_4		MOSI_2	SDA_4	Rx2_2	CMPO		PWM3_2
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3		CL5	PWM0_3

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PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3		CL6	PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3		CL7	PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3		CL8	PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0							OPO1	AIO8	
PT3.1							OPO2	DAO	
PT3.2								AIO4	
PT3.3								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
COM0			COM 0						
COM1			COM 1						
COM2			COM 2						
COM3			COM 3						
PT10.2			COM 4/SEG 0						
PT10.3			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						

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PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30	CS_8		Tx_8			PWM0_8
PT9.5			SEG 31	CK_8		Rx_8			PWM1_8
PT9.6			SEG 32	MISO_8		Tx2_8			PWM2_8
PT9.7			SEG 33	MOSI_8		Rx2_8			PWM3_8
PT10.0			SEG 34						
PT10.1			SEG 35						

Table 21-1 IO pin reuse functions and priority levels

21.2. Register address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO Base Address + 0x40(0x40840)	MASK1	GPIOMCR1	MASK0	GPIOMCR0
GPIO Base Address + 0x44(0x40844)	MASK3	GPIOMCR3	MASK2	GPIOMCR2
GPIO Base Address + 0x48(0x40848)	MASK5	GPIOMCR5	MASK4	GPIOMCR4
GPIO Base Address + 0x4C(0x4084C)	MASK7	GPIOMCR7	MASK6	GPIOMCR6

21.3. Register function

21.3.1. GPIO reuse function control register GPIOMCR0/ GPIOMCR1

GPIO Base Address + 0x40 (0x40840)								
Symbol	GPIOMCR0/ GPIOMCR1 (GPIO multiplex Control Register 0)							
Bit	[31:24]	[23:22]	[21]	[20]	[19]	[18]	[17]	[16]

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Name	MASK	-	-	-	PTCOPS	PTCOPE	-	PTCCPE
RW	R0W-0	-	-	-	RW-0	RW-0	-	RW-0
Bit	[15:08]	[7:5]		[4:2]			[1]	[0]
Name	MASK	PTCTC[2:0]		PTPW[2:0]			PTPW1E	PTPW0E
RW	R0W-0	RW-0						

Bit	Name	Description			
Bit[19]	PTCOPS	Rail-to-Rail OPAMP digital signal output port selection			
		0	Port 3.0		
		1	Port 3.1		
Bit[18]	PTCOPE	Rail-to-Rail OPAMP digital signal output port enable control			
		0	Disable, no output		
		1	Enable, output to the set target port		
Bit[16]	PTCCPE	Comparator output end IO port enable control			
		0	Disable, only used as a common IO, and no signal outputted		
		1	Enable		
Bit[7~5]	PTCTC	Capture comparator signal input end IO selection			
		000	Port 1.0 =TCI1	Port 1.1 =TCI2	Port 7.1 =TCI3
		001	Port 1.2 =TCI1	Port 1.3 =TCI2	Port 7.3 =TCI3
		010	Port 1.4 =TCI1	Port 1.5 =TCI2	Port 7.5 =TCI3
		011	Port 1.6 =TCI1	Port 1.7 =TCI2	Port 7.7 =TCI3
		100	Port 2.0 =TCI1	Port 2.1 =TCI2	Port 8.1 =TCI3
		101	Port 2.2 =TCI1	Port 2.3 =TCI2	Port 8.3 =TCI3
		110	Port 2.4 =TCI1	Port 2.5 =TCI2	Port 8.5 =TCI3
		111	Port 2.6 =TCI1	Port 2.7 =TCI2	Port 8.7 =TCI3
Bit[4~2]	PTPW	PWM output end IO port selection			
		000	Port 1.0 =PWM0	Port 1.1 =PWM1	
		001	Port 1.4 =PWM0	Port 1.5 =PWM1	
		010	Port 2.0 =PWM0	Port 2.1 =PWM1	
		011	Port 2.4 =PWM0	Port 2.5 =PWM1	
		100	Port 8.0 =PWM0	Port 8.1 =PWM1	
		101	Port 8.4 =PWM0	Port 8.5 =PWM1	
		110	Port 9.0 =PWM0	Port 9.1 =PWM1	
		111	Port 9.4 =PWM0	Port 9.5 =PWM1	
Bit[1]	PTPW1E	PWM 1 IO port input enable control			
		0	Disable (no output from the IO port)		
		1	Enable (the output port is set by the PTPW)		
Bit[0]	PTPW0E	PWM 0 IO port input enable control			

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		0	Disable (no output for the IO port)
		1	Enable (the output port is set by the PTPW)

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21.3.2. GPIO reuse function control register GPIOMCR2/ GPIOMCR3

GPIO Base Address + 0x44 (0x40844)					
Symbol	GPIOMCR2/ GPIOMCR3 (GPIO Multiplex Control Register 1)				
Bit	[31:24]	[23:20]		[19:17]	[16]
Name	MASK	-		I2CPTS	I2CPTEn
RW	R0W-0	-		RW-0	
Bit	[15:08]	[7:5]	[4]	[3:1]	[0]
Name	MASK	PTCSP	PTSPE	PTUR	PTURE
RW	R0W-0	RW-0			

Bit	Name	Description		
Bit[19~17]	I2CPTS	I2C communication IO port selection		
		000	Port 1.0 =SCL	Port 1.1 =SDA
		001	Port 1.2 =SCL	Port 1.3 =SDA
		010	Port 1.4 =SCL	Port 1.5 =SDA
		011	Port 1.6 =SCL	Port 1.7 =SDA
		100	Port 2.0 =SCL	Port 2.1 =SDA
		101	Port 2.2 =SCL	Port 2.3 =SDA
		110	Port 2.4 =SCL	Port 2.5 =SDA
		111	Port 2.6 =SCL	Port 2.7 =SDA
Bit[16]	I2CPTEn	I2C communication IO port reuse function enable control		
		0	Disable (no signal outputted)	
		1	Enable (the IO port is reused as the I2C communication port and the IO port is set by the I2CPTS)	
Bit[7~5]	PTCSP	SPI communication IO port selection		
		000	Port1.0 =CS, Port1.1 =CK, Port1.2 = MISO, Port1.3 =MOSI	
		001	Port1.4 =CS, Port1.5 =CK, Port1.6 = MISO, Port1.7 =MOSI	
		010	Port2.0 =CS, Port2.1 =CK, Port2.2 = MISO, Port2.3 =MOSI	
		011	Port2.4 =CS, Port2.5 =CK, Port2.6 = MISO, Port2.7 =MOSI	
		100	Port8.0 =CS, Port8.1 =CK, Port8.2 = MISO, Port8.3 =MOSI	
		101	Port8.4 =CS, Port8.5 =CK, Port8.6 = MISO, Port8.7 =MOSI	
		110	Port9.0 =CS, Port9.1 =CK, Port9.2 = MISO, Port9.3 =MOSI	
		111	Port9.4 =CS, Port9.5 =CK, Port9.6 = MISO, Port9.7 =MOSI	
Bit[4]	PTSPE	SPI communication IO reuse function enable control		
		0	Disable (only used as a common IO port)	
		1	Enable (The IO port is reused as the SPI communication port, and the communication IO port is set by the SPPTS.)	
Bit[3~1]	PTUR	UART communication IO port selection		
		000	Port 1.0 =TX	Port 1.1 =RX

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		001	Port 1.4 =TX	Port 1.5 =RX
		010	Port 2.0 =TX	Port 2.1 =RX
		011	Port 2.4 =TX	Port 2.5 =RX
		100	Port 8.0 =TX	Port 8.1 =RX
		101	Port 8.4 =TX	Port 8.5 =RX
		110	Port 9.0 =TX	Port 9.0 =RX
		111	Port 9.4 =TX	Port 9.5 =RX
Bit[0]	PTURE	EURAT communication IO reuse function enable control		
		0	Disable (only used as a common IO port)	
		1	Enable (The IO port is reused as the EUART communication port and the communication IO port is set by the PTUR.)	

MISO: Master input mode, Slave output mode.

MOSI: Master output mode, Slave input mode.

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21.3.3. GPIO reuse function control register GPIOMCR4/ GPIOMCR5

GPIO Base Address + 0x48 (0x40848)						
Symbol	GPIOMCR4/GPIOMCR5 (GPIO Multiplex Control Register 2)					
Bit	[31:16]					
Name	-					
RW	-					
Bit	[15:08]	[7:6]	[5]	[4:2]	[1]	[0]
Name	MASK	-	PTCI3E	PTPW2	PTPW3E	PTPW2E
RW	R0W-0	-	RW-0			

Bit	Name	Description		
Bit[5]	PTCI3E	TCI 3 mode control		
		0	The TCI3 is the same with the TC1.	
		1	The TCI3 configuration is set by the PTCTC.	
Bit[4~2]	PTPW2	PWM communication IO port selection		
		0	Port 1.2 =PWM2	Port 1.3 =PWM3
		1	Port 1.6 =PWM2	Port 1.7 =PWM3
		2	Port 2.2 =PWM2	Port 2.3 =PWM3
		3	Port 2.6 =PWM2	Port 2.7 =PWM3
		4	Port 8.2 =PWM2	Port 8.3 =PWM3
		5	Port 8.6 =PWM2	Port 8.7 =PWM3
		6	Port 9.2 =PWM2	Port 9.3 =PWM3
		7	Port 9.6 =PWM2	Port 9.7 =PWM3
Bit[1]	PTPW3E	GPIO PWM3 control switch		
		0	Disable	
		1	Enable	
Bit[0]	PTPW2E	GPIO PWM2 control switch		
		0	Disable	
		1	Enable	

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21.3.4. GPIO reuse function control register GPIOMCR6/ GPIOMCR7

GPIO Base Address + 0x4C (0x4084C)				
Symbol	GPIOMCR6/GPIOMCR7 (GPIO Multiplex Control Register 3)			
Bit	[31:16]			
Name	-			
RW	-			
Bit	[15:08]	[7:4]	[3:1]	[0]
Name	MASK	-	PTUR2	PTUR2E
RW	R0W-0	-	RW-0	

Bit	Name	Description		
Bit[3~1]	PTUR2	UART2 communication IO port selection		
		0	Port 1.2 = Tx2	Port 1.3 = Rx2
		1	Port 1.6 = Tx2	Port 1.7 = Rx2
		2	Port 2.2 = Tx2	Port 2.3 = Rx2
		3	Port 2.6 = Tx2	Port 2.7 = Rx2
		4	Port 8.2 = Tx2	Port 8.3 = Rx2
		5	Port 8.6 = Tx2	Port 8.7 = Rx2
		6	Port 9.2 = Tx2	Port 9.3 = Rx2
		7	Port 9.6 = Tx2	Port 9.7 = Rx2
Bit[5]	PTCI3E	GPIO UART2 control switch		
		0	Disable	
		1	Enable	

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22. ΣΔ 24-BIT A/D CONVERTER (ADC)

22.1. Overall description

The chip has an embedded high-performance 24-bit A/D converter (24-bitΣΔADC). The ADC has a pre low-noise programmable gain amplifier (Low Noise PGA), which can be used to amplify input signals. The gain programmable setting range is 1~128. The sampling rate of the ADC can be programmed by the register. The designed sampling rate is 350KHZ per second. It has a 3-stage regulator for filtering the quantized noise of the regulator. The programmable range of the over-sampling rate of the ADC is 32~32768. It is designed to measure the sensors with extremely small signals, such as strain meter, pressure gauge and industry process control.

Features:

The settable sampling rate is 40KHZ~350KHZ;
The resolution of the effective number (ENOB) of bits is up to 21 bits;
The lowest input noise is 65nV RMS;
The settable over-sampling rate is 32~32768;
The highest output rate is 10 KHz;
The multiplier gain of the built-in low-noise programmable gain amplifier is 1~128;
Built-in temperature sensor is provided;
Built-in 4-bit DAC is provided to adjust the offset;
3-stage comb filter is provided.

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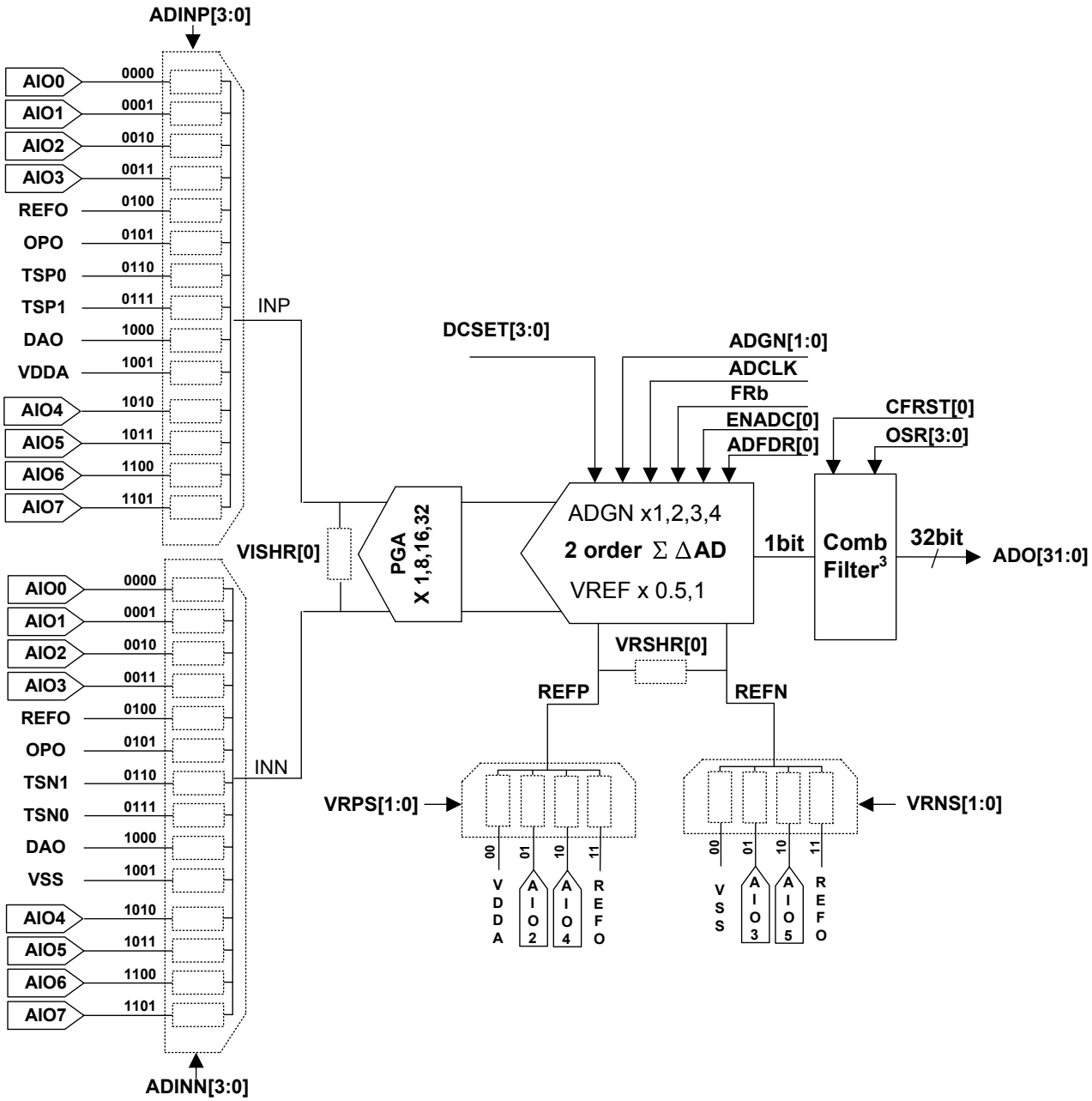
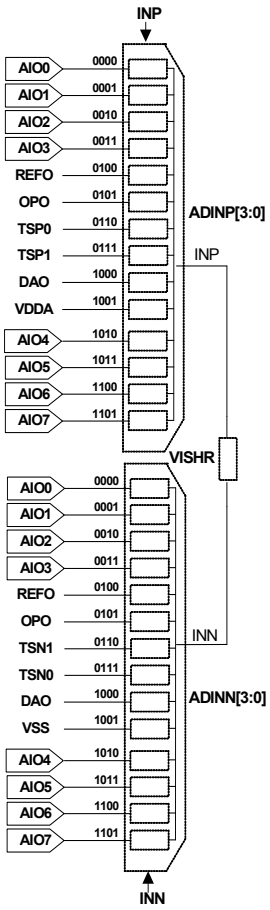


FIG. 22-1　ADC function block diagram

22.1.1. Fully differential signal input end

The input signal of the ADC is fully differential input mode; in other words, the input end is composed of the positive input end and the negative input end. The positive and negative signal input channels comprises 4 external signal input channels and 6 internal signal input channels. When the magnifying power of the ADC is 1, the input impedance of the signal input end of the ADC is 200K. The positive and negative signal input channels can be selected via the controllers ADINP[3:0] and ADINN[3:0]; however, the positive input end can only select one signal input channel at a time, and the negative input end can only select one signal input channel at a time. The positive and negative input ends can select the same input channel; in this way, the differential signal is close to 0 and only the offset is left. The ADC has an internal signal input channel short-circuit switch; the positive and negative the input ends can be set short-circuit via the control bit VISHR. The following figure lists the signal input channels of the positive and negative ends.



ADINP[3:0]	Positive input channel	ADINN[3:0]	Negative input channel
0000	AIO0	0000	AIO0
0001	AIO1	0001	AIO1
0010	AIO2	0010	AIO2
0011	AIO3	0011	AIO3
0100	REFO	0100	REFO
0101	OPO	0101	OPO
0110	TSP0	0110	TSN1
0111	TSP1	0111	TSN0
1000	DAO	1000	DAO
1001	VDDA	1001	VSS
1010	AIO4	0110	AIO4
1011	AIO5	0111	AIO5
1100	AIO6	1000	AIO6
1101	AIO7	1001	AIO7

FIG. 22-2 ADC signal input channel

The input signal is internally amplified and transferred, so the voltage range of the input signal is also limited. So as to obtain high resolution and linearity of the ADC outputs, it is suggested the differential voltage of the input signal beΔSI=±0.9*ΔVREF(ΔSI=INP-INN). The input signal voltages are as shown in the following table.

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External input channel	Voltage input range
ADINP	VSS-0.2V ≦ INP ≦ VDDA
ADINN	VSS-0.2V ≦ INN ≦ VDDA

Table 22-1 Input signal voltage range table

22.1.2. Built-in gain amplifier

The ADC has two built-in gain amplifiers: one is the low-noise, low temperature coefficient programmable gain amplifier PGA whose magnifying power is 8/16/32; the other one is the programmable gain amplifier ΣAD whose magnifying power is 1, 2 and 4. Thus, the maximal magnifying power of the combination of the two gain amplifiers is 128. However, the magnifying power is in inverse proportion to the effective number of bits (ENOB) of the ADC output; if the magnifying power is larger, the ENOB will be smaller. Thus, the magnifying power should be set according to the actual requirements. The magnifying power of the PGA can be set by the controller PGA[2:0], and the selection of the magnifying power of the PGA is as shown in the following table. The magnifying power of the ADC modulator can be set by the controller ADGN[1:0], and the selection of the magnifying power of the ADC modulator is as shown in the following table.

	PGA					ADC Modulator			
PGA[2:0]	000	001	011	111	ADGN[1:0]	00	01	10	11
Magnifying power	Disable	x 8	x16	x32	Magnifying power	x1	x2	RSV	x4

Table 22-2 Internal gain magnifying power

22.1.3. Reference voltage input channel

The reference voltage input of the ADC is fully differential input mode; in other words, the reference voltage input end is composed of the positive input end and negative input end. Both of the positive input end and negative input end respectively have two external input channels and two internal input channels. The positive input end can only select one input channel at a time, and the negative input end can only select one input channel at a time. The reference voltage end further has a short-circuit switch and the short-circuit switch can be enabled or disabled by the control bit VRSHR to achieve the short circuit between the positive input end and the negative input end.

The reference voltage can be generated after the ΔVREF voltage difference generated after the inputs from the VREFP and VREFN and then pass the programmable reference voltage attenuator. The attenuation power of the reference voltage can be set by the controller FRb[0], and the attenuation power of the reference voltage is as shown in the

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following table.

The calculation of the reference voltage is as follows:

ΔVREF=VREFP-VREFN (Equation 22-1)

VREF=Gain x ΔVREF (Equation 22-2)

ΔVREF: the voltage difference of the reference voltage; VREF: the internal reference voltage of the ADC

VREFP/VREFN: input reference voltage

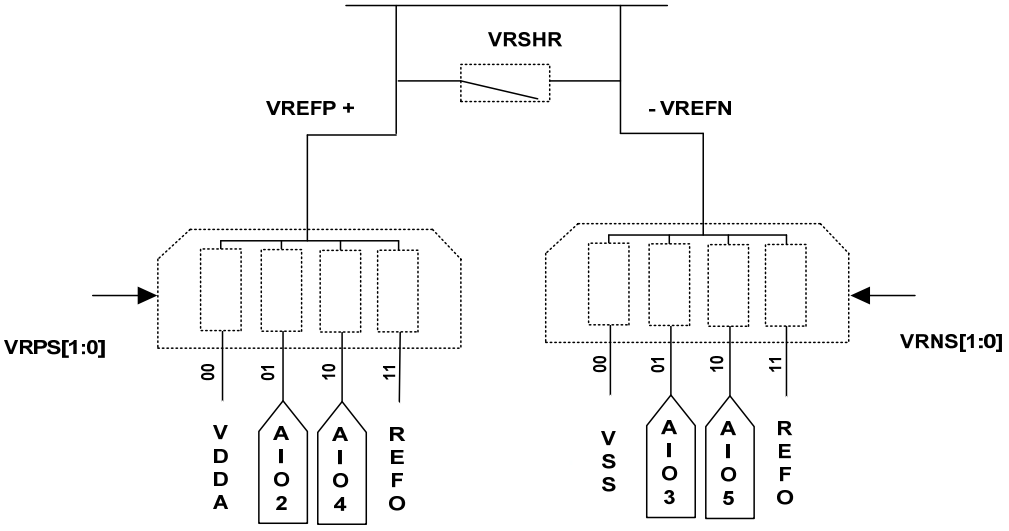

FIG. 18-3 Reference voltage input channel

Reference voltage attenuation power		
FRb[0]	0	1
Gain	1	1/2

Table 22-3 Reference voltage attenuation power

The input impedance of the positive input channels and the negative input channels is 500kΩ, and the input voltage of the VREFP or VREFN cannot be lower than the VSS and VDDA; if it is set as external input channel by the controller, the input impedance can be increased. However, it is necessary to pay attention to the voltage range of the external input channel.

In order to obtain the high resolution and linearity of the ADC output, it is suggested that the reference voltage ΔVREF=0.8V~1.8V.

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External input channel	Voltage input range
AIO2 / AIO4	VSS ≦ VREFP ≦ VDDA
AIO3 /AIO5	VSS ≦ VREFN ≦ VDDA

Table 22-4 Voltage input range of reference voltage external input channel

22.1.4. Input bias of input signal

The ADC has a zero point bias translation controller, and the zero point bias translation controller DCSET[3:0] can change the position of the zero point of the signal to prevent the voltage of the input signal from being too high to exceed the maximal measurement range. After the signal to be measured adjusted via the pre PGA, the ADC modulator and the zero point bias translation, the calculation formula of the equivalent signal to be measured ΔSI_I is as follows:

ΔSI_I = PGA x ADGN x ΔSI± +(DCSET x ΔVREF) (Equation 18-3)

	DCSET[3:0]							
Setting value	0000	0001	0010	0011	0100	0101	0110	0111
Translation value	0*VREF	+1/8* VREF	+1/4* VREF	+3/8* VREF	+1/2* VREF	+5/8* VREF	+3/4* VREF	+7/8* VREF
Setting value	1000	1001	1010	1011	1100	1101	1110	1111
Translation value	0*VREF	-1/8* VREF	-1/4* VREF	-3/8* VREF	-1/2* VREF	-5/8* VREF	-3/4* VREF	-7/8* VREF

Table 22-5 Zero bias configuration conversion table of input signal to be measured

22.1.5. Comb filter

ΣΔADC adopts the 3-stage comb filter, and different over-sampling rates can be obtained by setting the controller OSR[3:0] and the different combinations of the sampling rates of the ADC so as to realize different ADC conversion output frequencies. The configuration parameters of the OSR[3:0] are as follows:

	OSR[3:0]										
Setting value	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
Frequency dividing value	32768	16384	8192	4096	2048	1024	512	276	128	64	32

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Table 22-6　Frequency dividing table of over-sampling rates

The A/D conversion results are stored in the register ADCO[23:0], and the highest bit is the symbol bit, so the relations of the conversion results and the input signals are as shown in the following table.

2-polarity output 2's complement format	Equivalent signals to be measured	ADCO[23:0]	
		Hexadecimal system	Binary system
	ΔVR	7F FF FF	0111-1111 1111-1111 1111-1111
	ΔVR*(1/2	00 00 01	0000-0000 0000-0000 0000-0001
		00 00 00	0000-0000 0000-0000 0000-0000
	-ΔVR	FF FF FF	1111-1111 1111-1111 1111-1111
	ΔVR	80 00 00	1000-0000 0000-0000 0000-0000

Table 22-7　Relation table of ADCO[23:0] and input signals

The comb filter provides the reset control function; when the control bit CFRST is set as <0>, the comb filter will be reset, and then the comb filter will be enabled by setting the CFRST=1.　In this way, the ΣΔADC will automatically throw the first three pieces of data. When the user is waiting for the interrupt taking place, the first piece of the ADC conversion data which is read is the effective ADC value.

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22.1.6. Temperature sensor TPS

The temperature sensor is composed of a bipolar junction transistor, etc., and the change of the voltage signal to the temperature has passed the 0°K curve; thus, it has the following features:

When the environmental temperature is 0°K, the output voltage of the temperature sensor is V--tps@0°k = 0V;

The asymmetry between the offset voltage (VADC-OFFSET) of the ADC and the BJT can be automatically cancelled by the measuring;

The temperature calibration only needs single point calibration to satisfy the ±2℃error;

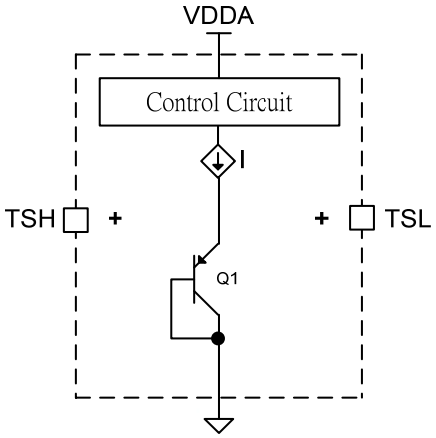

FIG. 22-4 Temperature sensor application block diagram

The TPS initialization configuration and calculation method are as follows:

Enable the ADC and the function of the TPS can be automatically enabled right away.

Fix the related configuration of the ADC and the system operating frequencies, and the configurations for the TPS calibration and measurement should be the same with each other.

When it is under the same temperature Ta(°C) and the values of the VTSH0 / VTSL0 and VTSH1 / VTSL1 are measured, add the two values and calculate the average to obtain the corresponding voltage VTS@Ta of the TPS under the temperature Ta.

When measuring the VTSH0 / VTSL0, set the INxP[3:0] as <0111> and set the INxN[3:0] as <0110>.

When measuring the VTSH1 / VTSL1, set the INxP[3:0] as <0110> and set the INxN[3:0] as <0111>.

Calculate the 2’s complement of the VTSH1 / VTSL1 add which to the values of the VTSH0 / VTSL0 and then divide which by 2 to obtain the VTS@Ta.

The variation of the output voltage VTS of the TPS to the temperature is a linear curve;

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therefore, the gain GTS can be derived (or slope).

$$G_{TS} = \frac{V_{TS@Ta} - V_{TS@0^{\circ}K}}{273.15 + T_{offset} + Ta} = \frac{V_{TS@Ta}}{289 + Ta} \quad \text{.....(Equation 22-4)}$$

G_{TS}：TPS 傳感器的增益或斜率
V_{TS}：TPS 傳感器的電壓
Ta：環境溫度
$^{\circ}K$：絕對溫度

The gain or slope of the TPS sensor
The voltage of the TPS sensor
Environmental temperature
Absolute temperature

TPS model description

If the temperature calibration point is Ta＝25℃＝298.15°K.
Configuration 1: the measurement result is VTSP@25℃＝52.515mV.....(1)
Configuration 2: the measurement result is VTSN@25℃＝-53.626mV.....(2)
((1)－(2)) ÷ 2 to obtain ΔVTS@27℃＝53.0705mV
∵VTS@0°K＝0.0mV
∴The curve slope is GTS＝(VTS@298.15°K－VTPS@0°K)÷(298.15－(0))≒178uV/°K.
Thus, the temperature of any points is T(°C)＝(VTS@T ÷GTS)－285.

22.1.7. ADC operation description

The ADC is the Δ-Σ structure of 24-bit resolution. If the user wants to enable the functions of the ADC, some peripheral circuits should be correct set. The power supply of the ADC is the VDDA voltage. Thus, the VDDA should be higher than 2.4V. If the user wants to better the performance of the ADC, a stable VDDA power supply is a must. As the VDDA needs some time to get ready, the ADD should start the measurement after the VDDA is ready. The offset and BandGap voltages can be enabled by setting the ENBGR is 1. Nest, it still needs a 1.2V common mode voltage to enable the ADC. The common mode voltage can be selected from the inside or outside. The ADC also needs a clock input whose maximum is 350 KHz. The inputted clock should be set to be higher than 40 KHz.

The detailed configuration and operation are as follows:

(1) Set and enable the operating clock source of the ADC, it is suggested that the sampling frequency of the ADC is set to be about 330khz;

Enable the VDDA voltage and the BandGap reference voltage, common mode reference

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voltage (REFO) and analog ground source, and the wait until the voltages are stable;
Select the input channels of the signals to be measured of the ADC, including positive, negative channels and turn off the input short-circuit switch;
Set the internal magnifying power of the ADC according to the actual conditions to make the ΔSI within 0.9*VREF;
Set the zero point bias DCSET; if it is not necessary, please set 0* VREF;
Select the reference voltage input channel of the ADC, turn off the input short-circuit switch and select the reference voltage attenuation rate;
Set the over-sampling frequency dividing value OSR[3:0] according to the actual ENOB;
Enable the ADC interrupt function according to the actual requirements and enable the global interrupt GIE;
Enable the ADC;
Reset the comb filter CFRST=0, and enable the comb filter CFRST=1; the hardware automatically throws the first 3 pieces of the data and then waits until the first ADC interrupt signal occurs; after that, the output data ADCO[23:0] of the ADC can be sampled.

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22.2. Register address

ADC Register Address	31	24	23	16	15	8	7	0
ADC Base Address + 0x00 (0x41100)	MASK0		REG0		MASK1		REG1	
ADC Base Address + 0x04 (0x41104)	REG2		REG3		MASK4		REG4	
ADC Base Address + 0x08 (0x41108)	ADO3		ADO2		ADO1		0x00	

-Reserved

22.3. Register function

22.3.1. Analog ADC register ADCCR0

ADC Base Address + 0x00 (0x41100)						
Symbol	ADCCR0 (ADC Control Register 0)					
Bit	[31:24]	[23:22]	[21]	[20]	[19:18]	[17:16]
Name	MASK	-	VISHR	VRSHR	VRPS	VRNS
RW	R0W-0	-	RW-0			
Bit	[15:08]	[7]	[6]	[5:2]	[1]	[0]
Name	MASK	-	ADFDR	OSR	CFRST	ENADC
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[21]	VISHR	ADC signal input end (positive and negative) short-circuit switch control	
		0	Short-circuit switch opens.
		1	Short-circuit switch closes.
Bit[20]	VRSHR	ADC reference voltage input end (positive and negative) short-circuit switch control	
		0	Short-circuit switch opens.
		1	Short-circuit switch closes.
Bit[19~18]	VRPS	Reference voltage positive input source selection	
		00	VDDA
		01	AIO2
		10	AIO4
		11	Reference buffer output(REFO)
Bit[17~16]	VRNS	Reference voltage negative input source selection	
		00	VSS
		01	AIO3
		10	AIO5
		11	Reference buffer output(REFO)
Bit[06]	ADFDR	Fast chopper stable mode configuration	
		0	Normal mode, the frequency of the chopper = ADCLK/128
		1	Fast chopper mode, the frequency= ADCLK/32, suitable for OSR<512

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Bit[5~2]	OSR	ADC over-sampling output frequency configuration (on the condition that the clock source of the ADC is 327680Hz)		
		0000	32768	Data output frequency 10sps
		0001	16384	Data output frequency 20sps
		0010	8192	Data output frequency 40sps
		0011	4096	Data output frequency 80sps
		0100	2048	Data output frequency 160sps
		0101	1024	Data output frequency 320sps
		0110	512	Data output frequency 640sps
		0111	276	Data output frequency 1280sps
		1000	128	Data output frequency 2760sps
		1001	64	Data output frequency 5120sps
		1010	32	Data output frequency 10240sps
		1011	Reserved (32768)	
		1100	Reserved (32768)	
		1101	Reserved (32768)	
		1110	Reserved (32768)	
		1111	Reserved (32768)	
Bit[01]	CFRST	Comb filter enable control		
		0	Reset (Level reset)	
		1	Enable	
Bit[00]	ENADC	ADC enable control		
		0	Disable	
		1	Enable	

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22.3.2. Analog ADC register ADCCR1

ADC Base Address + 0x04 (0x41104)							
Symbol	ADCCR1 (ADC Control Register 1)						
Bit	[31:29]	[28]	[27:24]	[23:22]	[21:20]	[19]	[18:16]
Name	-	Reg	DCSET	-	ADGN	FRb	PGA
RW	-	RW-0	RW-0	-	RW-0		
Bit	[15:08]			[7:4]		[3:0]	
Name	MASK			ADINP[		ADINN	
RW	R0W-0			RW-0			

Bit	Name	Description	
Bit[27~24]	DCSET	DC zero point translation input voltage selection (VREF = REFP-REFN)	
		0000	0 VREF
		0001	+1/8 VREF
		0010	+1/4 VREF
		0011	+3/8 VREF
		0100	+1/2 VREF
		0101	+5/8 VREF
		0110	+3/4 VREF
		0111	+7/8 VREF
		1000	0 VREF
		1001	-1/8 VREF
		1010	-1/4 VREF
		1011	-3/8 VREF
		1100	-1/2 VREF
		1101	-5/8 VREF
		1110	-3/4 VREF
		1111	-7/8 VREF
Bit[21~20]	ADGN	ADC input signal magnifying power Gain adjustor configuration	
		00	Gain = 1
		01	Gain = 2
		10	Reserved
		11	Gain = 4
Bit[19]	FRb	Reference voltage range selection	
		0	Full reference voltage input; it is VREF*1
		1	1/2 reference voltage input; VREF*1/2
Bit[18~16]	PGA	ADC input signal magnifying power PGA adjustor configuration	
		000	Gain = 1

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		001	Gain = 8
		010	Reserved
		011	Gain = 16
		100	Reserved
		101	Reserved
		110	Reserved
		111	Gain = 32
Bit[7~4]	ADINP	ADC positive signal input end selection	
		0000	AIO0
		0001	AIO1
		0010	AIO2
		0011	AIO3
		0100	REFO
		0101	OPO
		0110	TSP0
		0111	TSP1
		1000	DAO
		1001	VDDA
		1010	AIO4
		1011	AIO5
		1100	AIO6
		1101	AIO7
		1110	Reserved
		1111	Reserved
Bit[3~0]	ADINN	ADC negative signal input end selection	
		0000	AIO0
		0001	AIO1
		0010	AIO2
		0011	AIO3
		0100	REFO
		0101	OPO
		0110	TSN1
		0111	TSN0
		1000	DAO
		1001	VSS
		1010	AIO4
		1011	AIO5

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		1100	AIO6
		1101	AIO7
		1110	Reserved
		1111	Reserved

22.3.3. Analog ADC register ADCCR2

ADC Base Address + 0x08 (0x41108)		
Symbol	ADCCR2 (ADC Control Register 2)	
Bit	[31:16]	
Name	ADCO	
RW	R-0	
Bit	[15:8]	[7:0]
Name	ADCO	RSV
RW	R-0	R-0

ADCO[31:0] ADC transformed value output register; only data higher than 24-bit are effective.

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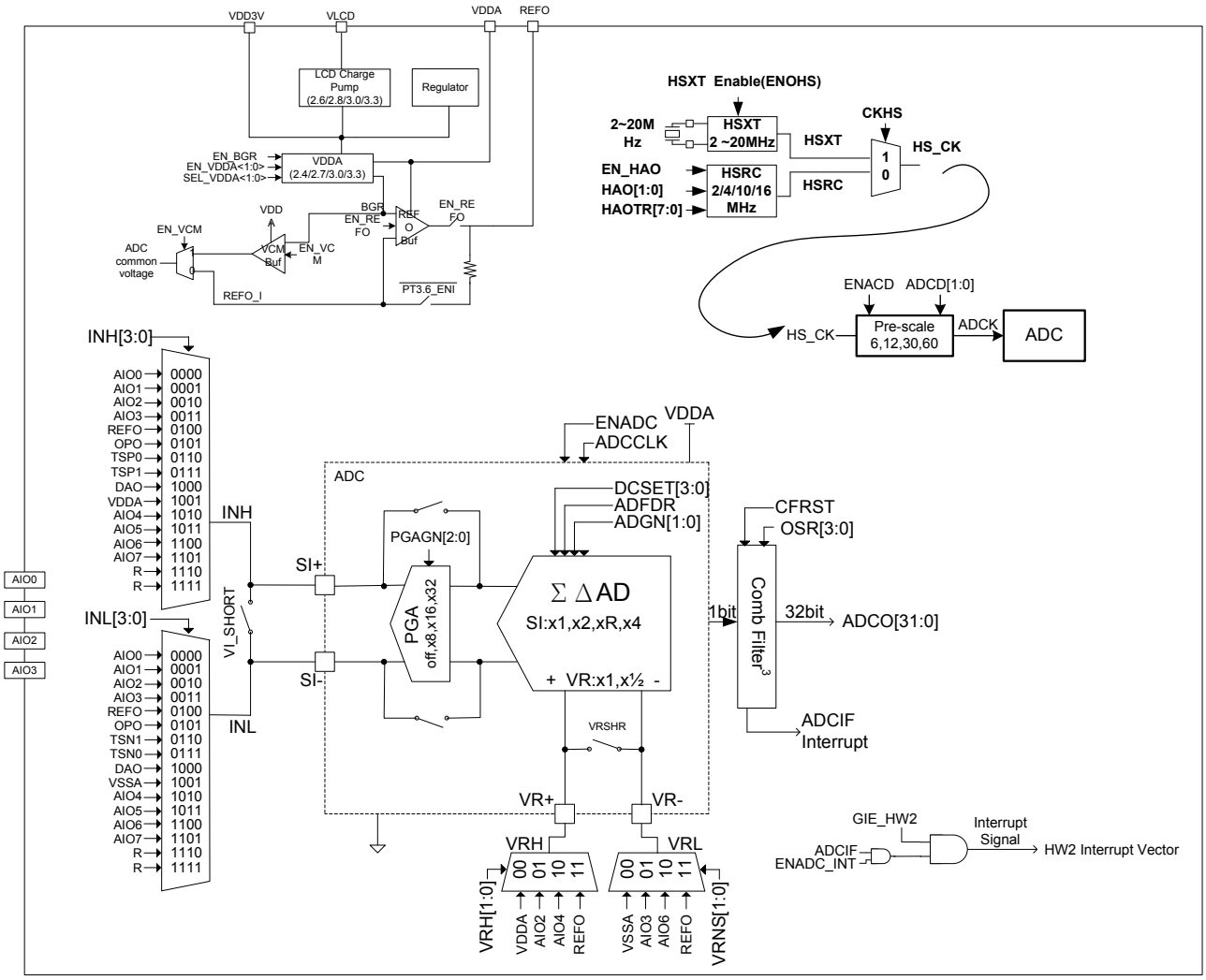
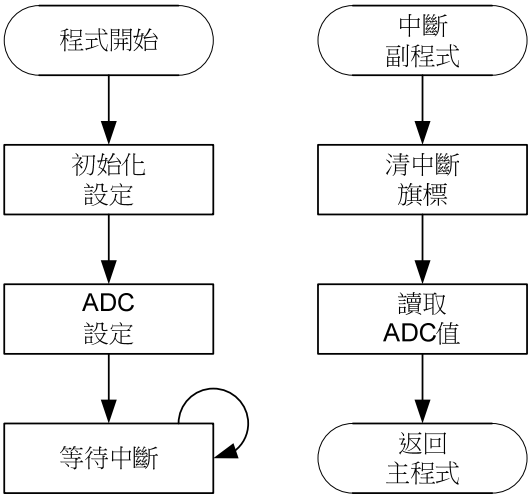
22.4. Model program flow





The program starts.

Initialization settings

ADC settings

Wait for interrupt

Interrupt the subprogram
Clear the interrupt flag
Reverse the value of the ADC
Return to the main program

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22.5. Model program function

Model name: The ADC interrupt usage method

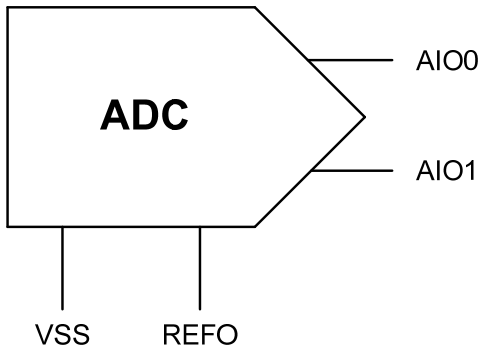
The ADC interrupt function can be realized by the related configuration of the ADC.

Set the powers of the ADC: VDDA and REFO.

Set the clock of the ADC: ADCCLK.

The Vin of the ADC is AIO0-AIO1.

The Vref of the ADC is REFO to VSS.



18.6Model program description

```
00
01  #include "HY16F19X.h"
02
03  unsigned int ADCData;
04
05  #define   Disable   0
06  #define   Enable    1
07
08  int main(void)
09  {
10  //Set ADC input pin
11
12    DrvADC_SetADCInputChannel(ADC_Input_AIO0,ADC_Input_AIO1); //Set ADC positive input AIO0
13                                                              //Set ADC negative input AIO1
14    DrvADC_InputSwitch(OPEN);                                 //ADC input short control
15    DrvADC_RefInputShort(OPEN);                               //ADC reference short control
16
17    DrvADC_Gain(ADC_PGA_Disable,ADC_PGA_Disable);             //Input signal gain
18
19    DrvADC_DCoffset(0);                                       //DC offset
20    DrvADC_RefVoltage(REF_BUFFER_OUT,VSSA);                   //ADC reference voltage.
21
22    DrvADC_FullRefRange(0);                                   //ADC full reference range select
23                                                              //0: Full reference range input
24                                                              //1: 1/2 reference range input
25
26
27
```

28		
29	//ADC Speed	
30		
31	DrvADC_OSR(1);	//1 : OSR=16384
32	DrvADC_CombFilter(Enable);	//Enable OSR
33		
34	DrvADC_ClkEnable(0,1);	//Setting ADC CLOCK
35		//ADCK=HS_CK/6
36		// Rising edge is high
37		
38	//Set VDDA voltage	
39		
40	DrvPMU_VDDA_Voltage(E_VDDA2_4);	//VDDA=2.4
41	DrvPMU_VDDA_LDO_Ctrl(E_LDO);	//LDO ON
42	DrvPMU_BandgapEnable();	
43	DrvPMU_REFO_Enable();	
44		
45	DrvPMU_AnalogGround(Enable);	//ADC analog ground source set
46		//1 : Enable buffer
47		//and use internal source
48		//need to work with ADC
49		
50	//Set ADC interrupt	
51		
52	DrvADC_EnableInt();	
53	DrvADC_ClearIntFlag();	
54	DrvADC_Enable();	
55		
56	SYS_EnableGIE(7);	//Enable GIE
57		
58	while(1);	//Wait for Interrupt
59		
60	}	
61		
62	void HW2_ISR(void)	//ADC interrupt
63	{	
64	DrvADC_ClearIntFlag();	//Clear ADC interrupt flag
65	ADCData=DrvADC_GetConversionData();	//Get ADC data
66	}	
67		

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23. RAIL-TO-RAIL OPAMP

23.1. Overall description

The chip has an embedded Rail-to-Rail OPAMP network, which is mainly used to deal with analog signals. The input range and the output range are from VSS to VDDA. When the input signal range is between VSS +0.1 V and VDDA - 0.1V, the open loop gain is higher than 80dB. When the output load is 50PF, the unit gain bandwidth is 1MHz. It has the 1mA input and output push-pull driving ability. The maximal drivable capacitor load is 100pF. The positive input end has 4 independent selection switches and the negative input end has 6 independent selection switches. The OPAMP network has a built-in 10pF capacitor. It can serve as input sampling capacitor or integrator. Different input channel configurations and 8-bit DAC configurations can achieve different applications. The output end of the OPAMP can be connected to an I/O pin, or used by other internal IPs. When it serves as comparator, its output is digital format. The user can set the output of the OPAMP to pass a 2us peak pulse filter. Besides, the output of the comparator can be on-and-off or opposite in phase.

The features of the OPAMP include:

Rail-to-Rail input range, and Rail-to-Rail output range;
Under a 2pF load, it can provide a 1MHz unit gain bandwidth and 60 phase margin;
The DC gain can be higher than 80dB;
1mA push-pull output driving ability;
The positive input end has 4 independent selection switches and the negative input end has 6 independent selection switches.
Built-in 10pF capacitor;
It can serve as comparator with the function of a chopper;
Built-in peak pulse digital low-pass filter;

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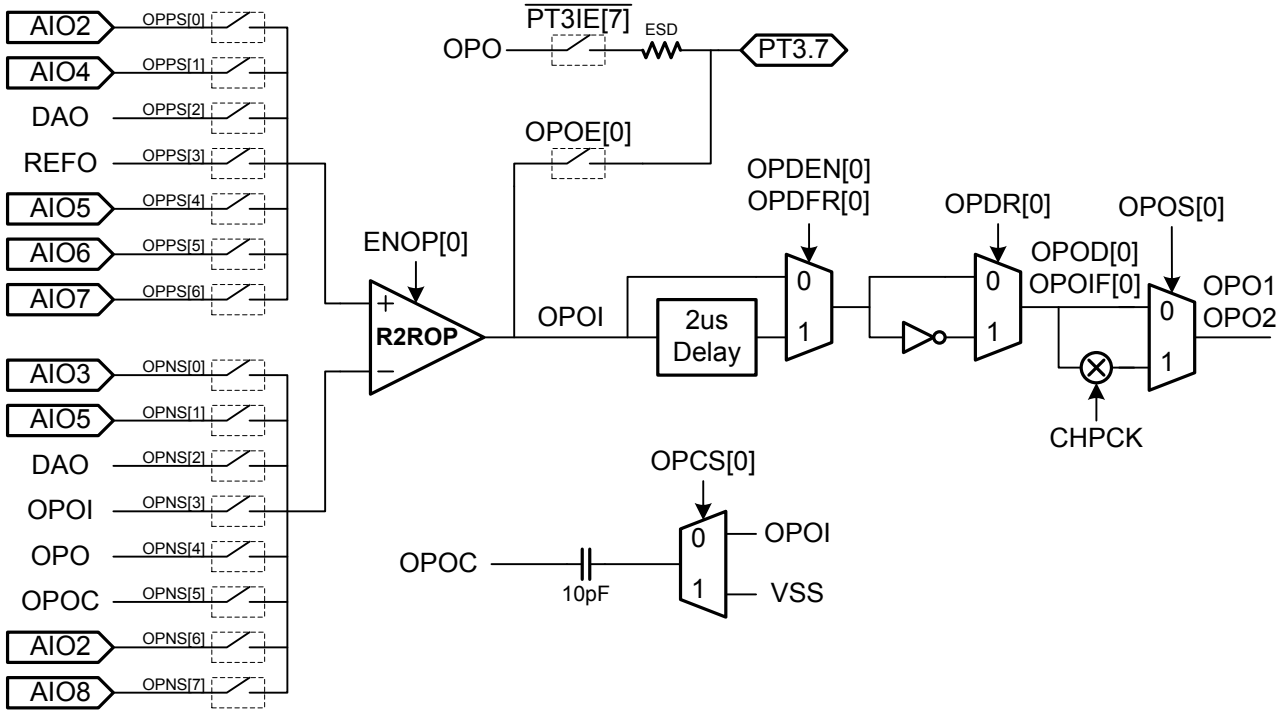

FIG. 23-1 OPAMP function block diagram

23.1.1. Input channel independent selection switch

The input channel selector of the OPAMP is not a multiplexer but an independent selection switch. The positive input channel of the OPAMP is controlled by 7 switches: AIO 2, AIO 4, DAO, REFO, AIO5, AIO6 and AIO7, which can be respectively controlled by the control bits OPPS[0], OPPS[1], OPPS[2], OPPS[3], OPPS[4], OPPS[5] and OPPS[6]; besides, multiple positive input channels can be selected at the same time. The negative input channel of the OPAMP is controlled by 8 switches: AIO3, AIO5, DAO OPOI, OPO, OPOC, AIO2 and AIO8, which can be respectively controlled by the control bits OPNS[0], OPNS[1], OPNS[2], OPNS[3], OPNS[4], OPNS[5], OPNS[6] and OPNS[7]; similarly, multiple negative input channels can be selected at the same time.

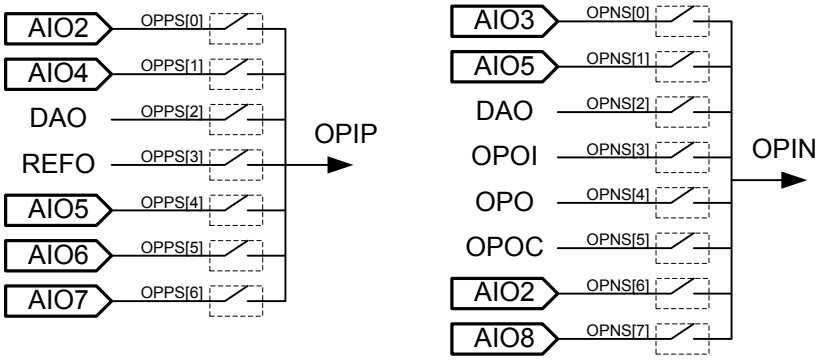

FIG. 23-2 Input channel configuration diagram

23.1.2. Built-in 10pF capacitor

The OPAMP has a built-in 10uF capacitor, which can have different functions under different configurations. The upper end of the capacitor is connected to the OPOC and can be connected to the negative input end; the switch is set by the control bit OPNS [6]; the lower end of the capacitor can be connected to the OPOI or VSS, which can be set by the control bit OPCS[0]. There are two methods to sample the analog inputs. One is the open loop sampling technique, and the method requires the analog signals are inputted from the AIO or AIO 5. The configuration of the channel switch is as follows: first, set the OPNS[5] as 1 and set the OPCS[0] as 1; then, set the OPNS [0]=1 (select the AIO3) or set the OPNS [1]=1 (select the AIO5); after the sampling is finished, ser the OPNS [5]=0; the voltage data are stored in the capacitor corresponding to the VSS. The other one is the close loop sampling technique: the method should enable the OPAMP first, which means setting the ENOP=1; then, enable the OPOI and OPO, which means setting the OPNS[4]=1 and OPNS[3]=1; afterward, the lower end of the capacitor is connected to the OPOI, which means the OPCS=1; enable the AIO2 and AIO 4, which means setting the OPPS[0]=1 and OPPS[1]=1; after the sampling is finished, disable the OPOC, which means setting the OPNS[5]=0; the voltage data are also stored in the capacitor corresponding to the VSS. The close loop method can store the offset of the OPAMP in

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the capacitor. Additionally, if the applications have the sensors with very high output impedance, the close loop sampling technique is a better choice. Finally, the lower end of the capacitor can be connected t the output end of the OPAMP, which means setting the OPCS=0. Meanwhile, the AIO3 and the AIO5 pins can be used to perform cumulative charge.

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23.1.3. Comparator function

If the configuration of the OPAMP is set as the open loop function, the OPAMP can serve as comparator. The 1-bit binary codes can be outputted by the OPOD. If the positive input is higher than the negative input, the OPOD outputs 1; if the positive input is smaller than the negative input, the OPOD outputs 0. In order to prevent from the peak pulse interference, the outputs of the OPOD can further pass the 2us low-pass filter. If any peak pulse is smaller than 2us, the outputs of the comparator will not change. The outputs of the comparator can be changed by setting the control bit OPDR.

The output of the comparator can be also connected to the I/O pins; The PT3.0/PT3.1 are respectively the output pins of the OPO1/OPO2. The output results of the comparators can further be multiplied by the clock frequency of the charge pump (CHPCK) to output a high-frequency signal, which can serve as the LED driver.

23.1.4. Operation description

The OPAMP is a more universal Rail-to-Rail OP amplifier. It can be used to deal with analog signals. When it is used as OP amplifier, the voltage of the VDDA is higher than 2.4V and the reference voltage of the BandGap should be enabled in advance. Within the effective input range, the OPAMP is Rail-to-Rail. However, in order to achieve better performance, it is suggested that the input common mode voltage range is between VSS+0.1V~VDDA-0.1V. The input impedance of the OPAMP is higher than 1GΩ.

Initialization configuration:

Enable the reference voltages of the VDDA and BandGap, the voltage of the VDDA should be higher than 2.4V, and wait until the voltages are stable.

Select the output pins of the OPO1/OPO2, and set the corresponding IO pins as the input mode. It is not necessary to set the above configuration if the above function is not used;

Select the positive input channel, negative input channel according to the actual applications;

Set the 2us low-pass filter and enable or disable it according to the actual requirements;

Set the clock frequency of the charge pump and determine whether it is multified by the frequency or not;

Enable the analog output of the OPAMP, which means enabling the OPOE;

Enable the digital output of the OPAMP according to the actual requirements, which means enabling the OPDEN;

If the digital output of the OPAMP is enabled, the output result should be set to be opposite in phase or not according to the actual requirements, which means setting the OPDR.

Enable the OPAMP to enable the OP amplifier, which means enabling the ENOP;

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23.2. Register address

OPAMP Register Address	31	24	23	16	15	8	7	0
OPAMP Base Address + 0x00 (0x41900)	-		-		MASK0		REG0	
OPAMP Base Address + 0x04 (0x41904)	OPPSM		OPPS		OPNSM		OPNS	

-Reserved

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23.3. Register function

23.3.1. Analog OPA register 0

OPA Base Address + 0x00 (0x41900)									
Symbol	OPAMP0 (OPAMP Control Register 0)								
Bit	[31:16]								
Name	RSV								
RW	R-0								
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	OPOD	OPOS	OPDR	OPCS	OPDFR	OPDEN	OPEO	ENOP
RW	R0W-0	R-0	RW-0						

Bit	Name	Description
Bit[7]	OPOD	OPAMP digital output value, read-only
		0 Negative input end signal > positive input end signal;
		1 Positive input end signal > Negative input end signal;
Bit[6]	OPOS	Set the outputs of the OPO1/OPO2 pass through the CPCLK multi-functioner.
		0 If the outputs fail to pass the CPCLK multi-functioner, the outputs of the OPO1/OPO2 are equivalent to the OPOD.
		1 If the outputs pass the CPCLK multi-functioner, the OPO1/OPO2 are equivalent to the OPOD+CPCLK.
Bit[5]	OPDR	OPAMP digital output phase selection
		0 Normal output
		1 Reverse output
Bit[4]	OPCS	OPAMP built-in capacitor purpose configuration
		1 The capacitor serves as integrated capacitor, and the lower end is connected to the OPOI.
		0 The capacitor serves as sampling capacitor, and the lower end is connected to the VSS.
Bit[3]	OPDFR	OPAMP output digital filter enable control
		0 Disable
		1 Enable (Pass through the 2us deglitch)
Bit[2]	OPDEN	OPAMP digital output function control
		0 Disable
		1 Enable
Bit[1]	OPEO	OPAMP analog output function control
		0 Disable
		1 Enable
Bit[0]	ENOP	OPAMP function enable control
		0 Disable
		1 Enable

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23.3.2. Analog OPA register 1

OPA Base Address + 0x04 (0x41904)			
Symbol	OPAMP1 (OPAMP Control Register 1)		
Bit	[31:24]	[23]	[22:16]
Name	MASK	-	OPPS[6:0]
RW	R0W-0	-	RW-0
Bit	[15:08]	[07:00]	
Name	MASK	OPNS[5:0]	
RW	R0W-0	RW-0	

Bit	Name	Description	
Bit[22]	OPPS[6]	OPAMP positive input channel 6	
		0	Disable, high impedance
		1	Enable and connect to the AIO7
Bit[21]	OPPS[5]	OPAMP positive input channel 5	
		0	Disable, high impedance
		1	Enable and connect to the AIO6
Bit[20]	OPPS[4]	OPAMP positive input channel 4	
		0	Disable, high impedance
		1	Enable and connect to the AIO5
Bit[19]	OPPS[3]	OPAMP positive input channel 3	
		0	Disable, high impedance
		1	Enable and connect to the REFO
Bit[18]	OPPS[2]	OPAMP positive input channel 2	
		0	Disable, high impedance
		1	Enable and connect to the DAO
Bit[17]	OPPS[1]	OPAMP positive input channel 1	
		0	Disable, high impedance
		1	Enable and connect to the AIO4
Bit[16]	OPPS[0]	OPAMP positive input channel 0	
		0	Disable, high impedance
		1	Enable and connect to the AIO2
Bit[7]	OPNS[7]	OPAMP negative input channel 7	
		0	Disable, high impedance
		1	Enable and connect to the AIO8
Bit[6]	OPNS[6]	OPAMP negative input channel 6	
		0	Disable, high impedance
		1	Enable and connect to the AIO2

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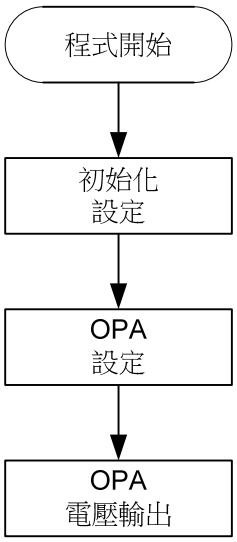
Bit[5]	OPNS[5]	OPAMP negative input channel 5	
		0	Disable, high impedance
		1	Enable and connect to the OPC: internal 10pF capacitor
Bit[4]	OPNS[4]	OPAMP negative input channel 4	
		0	Disable, high impedance
		1	Enable and connect to the OPOI: internal OPAMP output
Bit[3]	OPNS[3]	OPAMP negative input channel 3	
		0	Disable, high impedance
		1	Enable and connect to the OPO: internal OPAMP output
Bit[2]	OPNS[2]	OPAMP negative input channel 2	
		0	Disable, high impedance
		1	Enable and connect to the DAO
Bit[1]	OPNS[1]	OPAMP negative input channel 1	
		0	Disable, high impedance
		1	Enable and connect to the AIO5
Bit[0]	OPNS[0]	OPAMP negative input channel 0	
		0	Disable, high impedance
		1	Enable and connect to the AIO3

23.4. Model program flow



The program starts.

Initialization settings

OPA settings

OPA voltage output

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23.5. Model program function

Model name: The OPAMP usage and setting method

Enable the analog voltage REFO=1.2V.

Connect the REFO to the positive end V+ of the OPAMP.

Select the OPOI as the negative end of the OPAMP; now it will be the OPA Unit Gain Buffer.

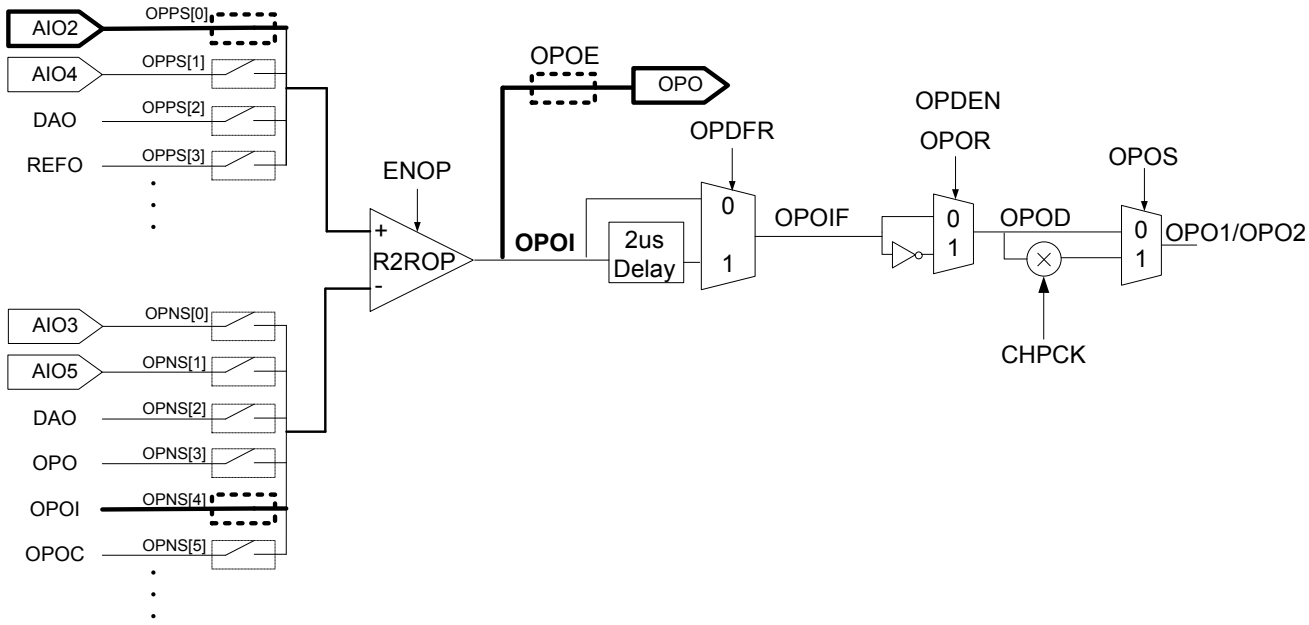
Via proper OPAMP network setting, the REFO=1.2V can be measured at the output end of the OPO.

23.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  int main(void)
04  {
05      DrvPMU_VDDA_LDO_Ctrl(E_LDO);              //LDO ON
06      DrvPMU_VDDA_Voltage(E_VDDA3_0);           //VDDA=3.0
07      DrvPMU_REFO_Enable();                     //REFO ON
08
09      DrvOP_Open();
10
11      DrvOP_PInput(0x08);                       //OPA positive reference input selection REFO
12      DrvOP_NInput(0x10);                       //OPA negative reference input selection OPOI
13
14      DrvOP_OPOoutEnable();                     //OP OoutEnable
15
16      while(1);                                 //while loop
17  }
18
```

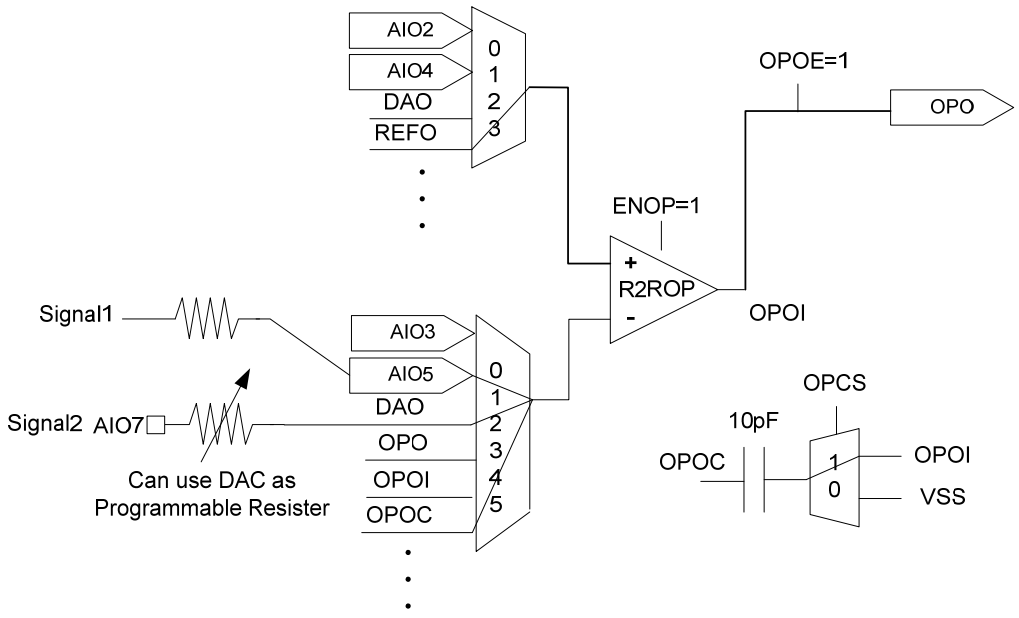
23.7. OPAMP application circuit system I

Use as a Unit Gain Buffer



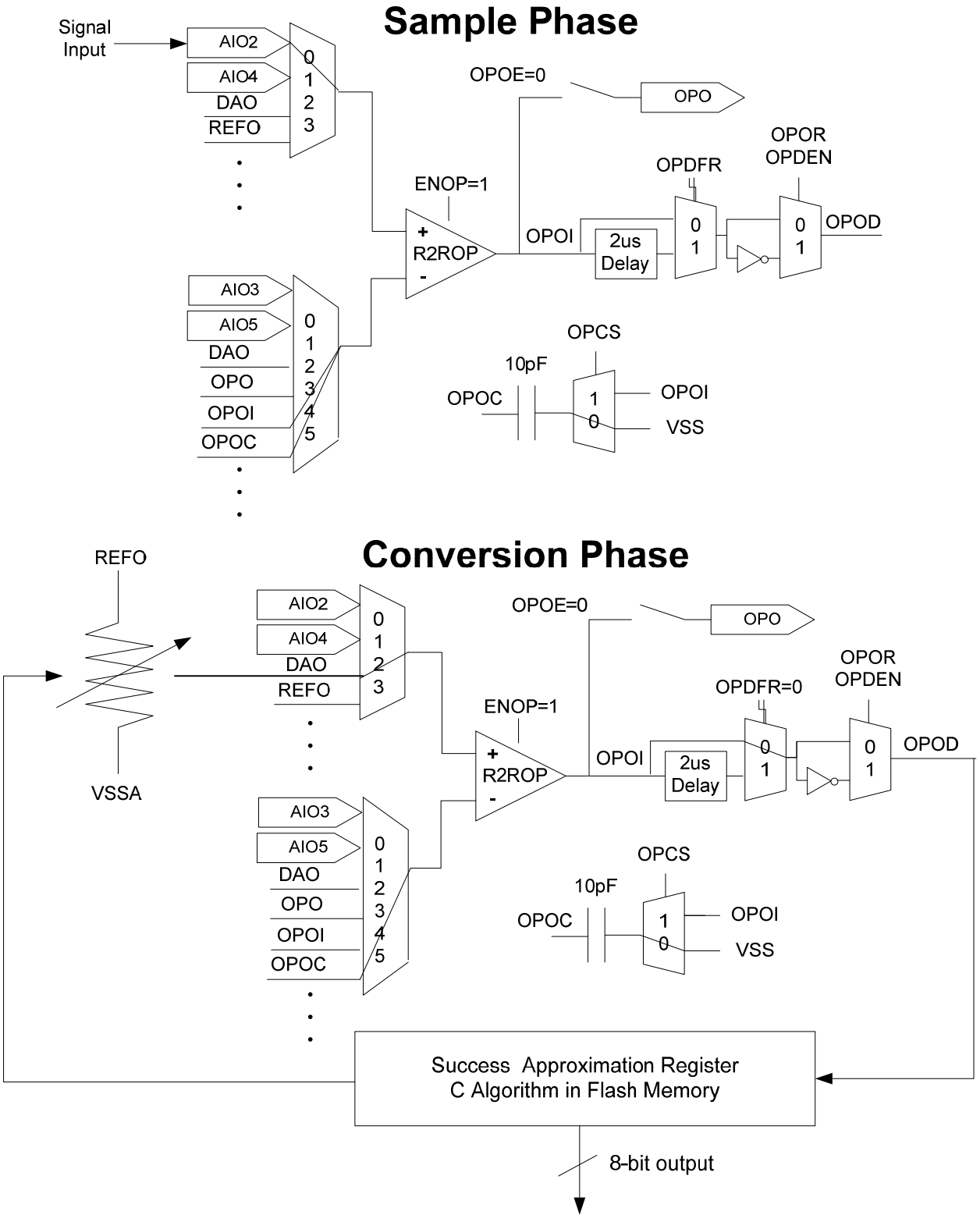
23.8. OPAMP application circuit system II

Use as an Integrator



23.9. OPAMP application circuit system III

Use as a 8-bit SAR ADC



24. A/D converter DAC

24.1. Overall description

The chip has an embedded 8-bit A/D converter DAC. The DAV8 module is an 8-bit A/D converter, which is composed of a step resistor with absolute monotonicity.

Features of DAC8 include:

8-bit monotonic output

Internal or external reference programmable selection

It can serve as programmable resistor.

Operation of DAC8:

When the ENDA is 0, the DAC8 will be disabled and no power consumption will be incurred. The Vrefp multiplexer is disabled and becomes a high impedance node. However, the Vrefn is still enabled, and connects to one of the sources. If the DAOE is set as 1, it will become a programmable resistor able to mark the ohm values.

DAC8 output:

The DA8 can generate the output voltages according to the data stored in the DABIT and VDA_Vrefp – VDA_Vrefn.

DABIT is based on straight binary system; the following figure is the transmission function diagram.

$$DAO = (V_{DAC\_Vrefp} - V_{DAC\_Vrefn}) \times \frac{DAbit\_in}{256} + V_{DAC\_Vrefn}$$

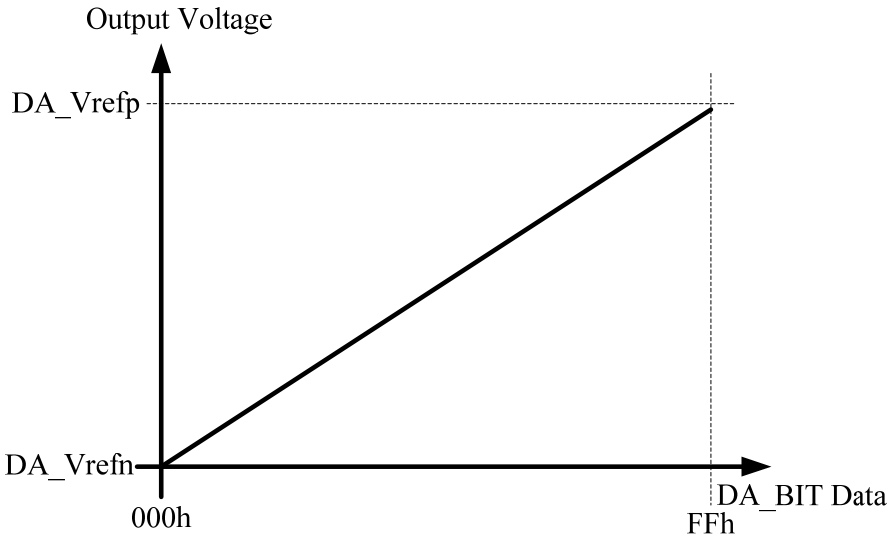


FIG. 24-1 DAC conversion diagram

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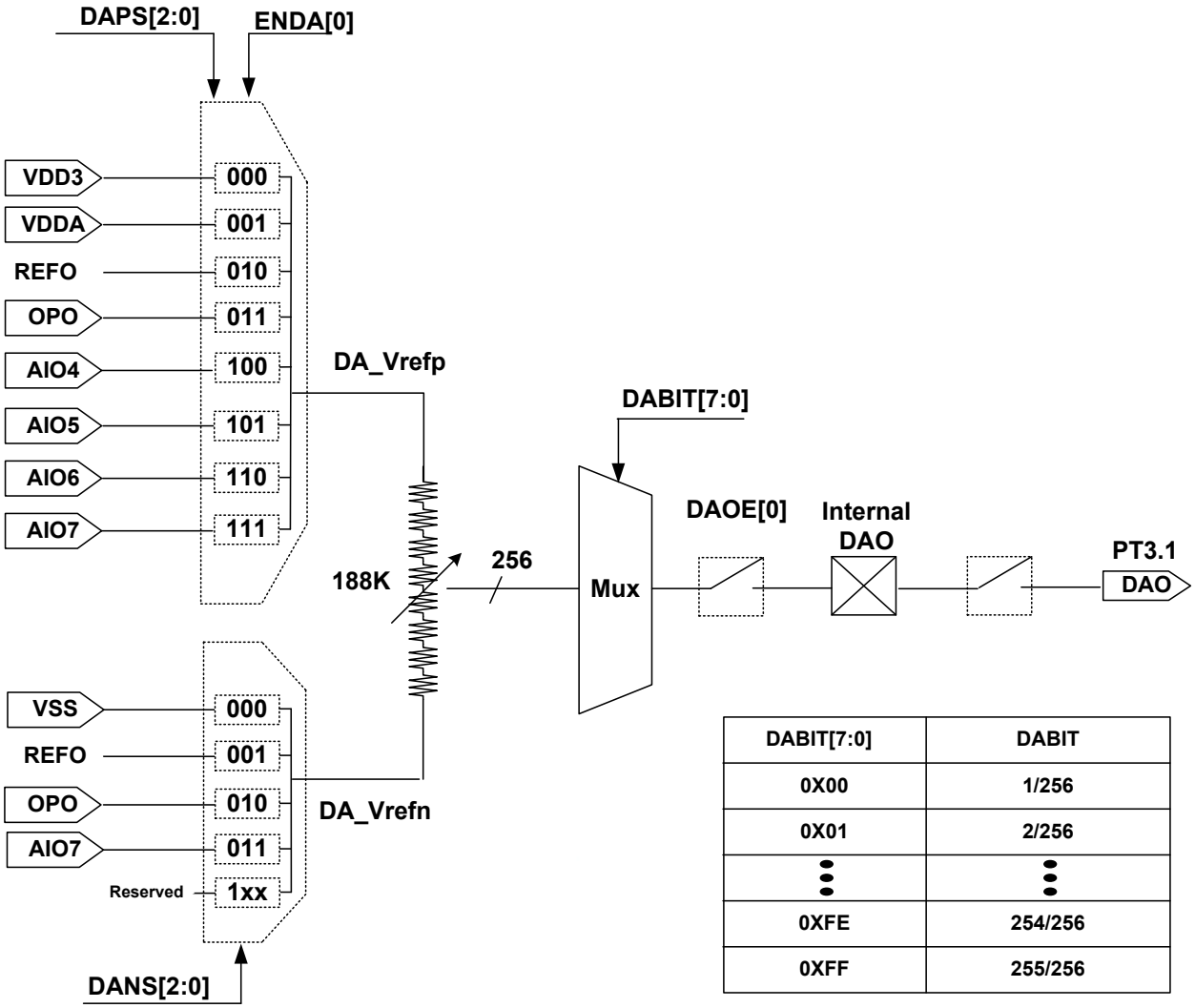

DABIT[7:0]	DABIT
0X00	1/256
0X01	2/256
⋮	⋮
0XFE	254/256
0XFF	255/256

FIG. 24-2 DAC function block diagram

24.2. Register address

DAC Register Address	31	24	23	16	15	8	7	0
DAC Base Address + 0x00 (0x41700)	-		-		MASK0		REG0	
DAC Base Address + 0x04 (0x41704)	-		-		MASK1		REG1	

-Reserved

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24.3. Register function

24.3.1. DAC register 0

DAC Base Address + 0x00 (0x41700)						
Symbol	DAC0 (DAC Control Register 0)					
Bit	[31:16]					
Name	RSV					
RW	R-0					
Bit	[15:8]	[7]	[6:4]	[3:2]	[1]	[0]
Name	MASK	DANS[2]	DAPS[2:0]	DANS[1:0]	DAOE	ENDA
RW	R0W-0	RW-0				

Bit	Name	Description	
Bit[5~4]	DAPS	DAC positive input source selection	
		000	VDD3V
		001	VDDA
		010	REFOI
		011	OPO
		100	AIO4
		101	AIO5
		110	AIO6
		111	AIO7
Bit[3~2]	DANS	DAC negative input source selection	
		000	VSS
		001	REFOI
		010	OPO
		011	AIO7
		100~111	Rsv
Bit[1]	DAOE	DAC output enable control.	
		0	Disable, under high impedance
		1	Enable, the DAC outputs corresponding voltage.
Bit[0]	ENDA	DAC function enable control	
		0	Disable
		1	Enable

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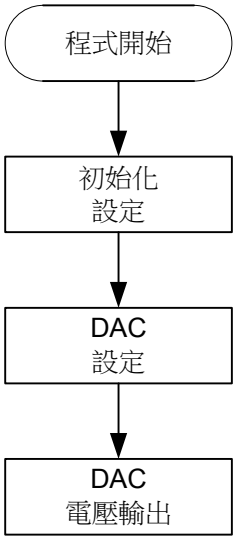
24.3.2. DAC register 1

DAC Base Address + 0x00 (0x41704)		
Symbol	DAC1 (DAC Control Register 1)	
Bit	[31:16]	
Name	RSV	
RW	R-0	
Bit	[15:8]	[7:0]
Name	MASK	DABIT[7:0]
RW	R0W-0	RW-0

Bit	Name	Description
Bit[7~0]	DAO	DAO[7:0] the ratio setting of the output voltage; that is DAO[7:0]/275.

24.4. Model program flow



The program starts.
Initialization settings
DAC settings
DAC voltage output

24.5. Model program function

Model name: DAC usage method and description

Model description:

Appropriately set the analog voltage and the digital voltage.
Connect the REFO to the positive end of the DAC.
Select the VSS as the negative end of the DAC, which will use the AIO4 of the OP. (The

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AIO4 and DAC should be selected together.)
256-stage DAC outputs can be measured at the output end of the AIO4 via proper DAC network setting.
Or adopt the DAC dedicated analog voltage output pin PT3.1.

24.6. Model program description

```
00
01  #include "HY16F19X.h"
02  int i;
03  int main(void)
04  {
05      DrvPMU_VDDA_LDO_Ctrl(E_LDO);                //LDO ON
06      DrvPMU_VDDA_Voltage(E_VDDA3_0);             //VDDA=3.0
07
08      DrvOP_PInput(E_DAC_PVDD3V);                 //DAO output with AIO4(PIN29)
09      DrvDAC_Enable();                            //DAC IP enable
10      DrvDAC_EnableOutput();                      //DAC output enable
11      DrvDAC_Open(1,0,0x10);                      //DAC_Vrefp= VDDA
12      DrvDAC_SetoutputIO(1);                      //DAC output with PT3.1
13      while(1);                                   //while loop
14  }
15
```

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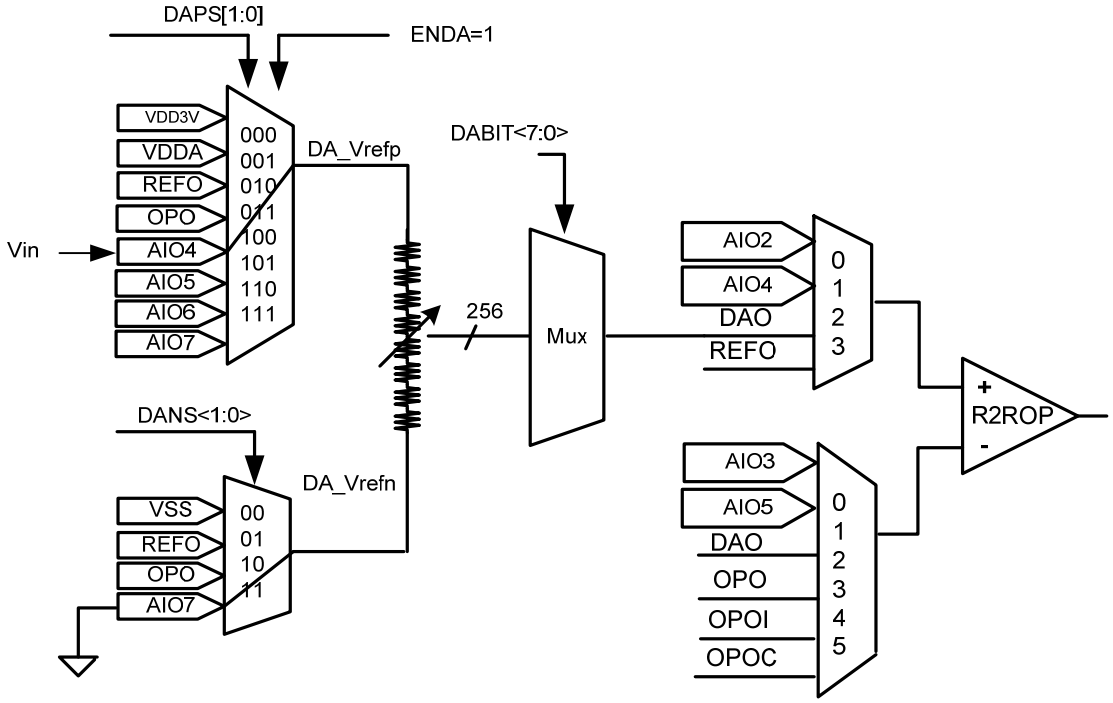
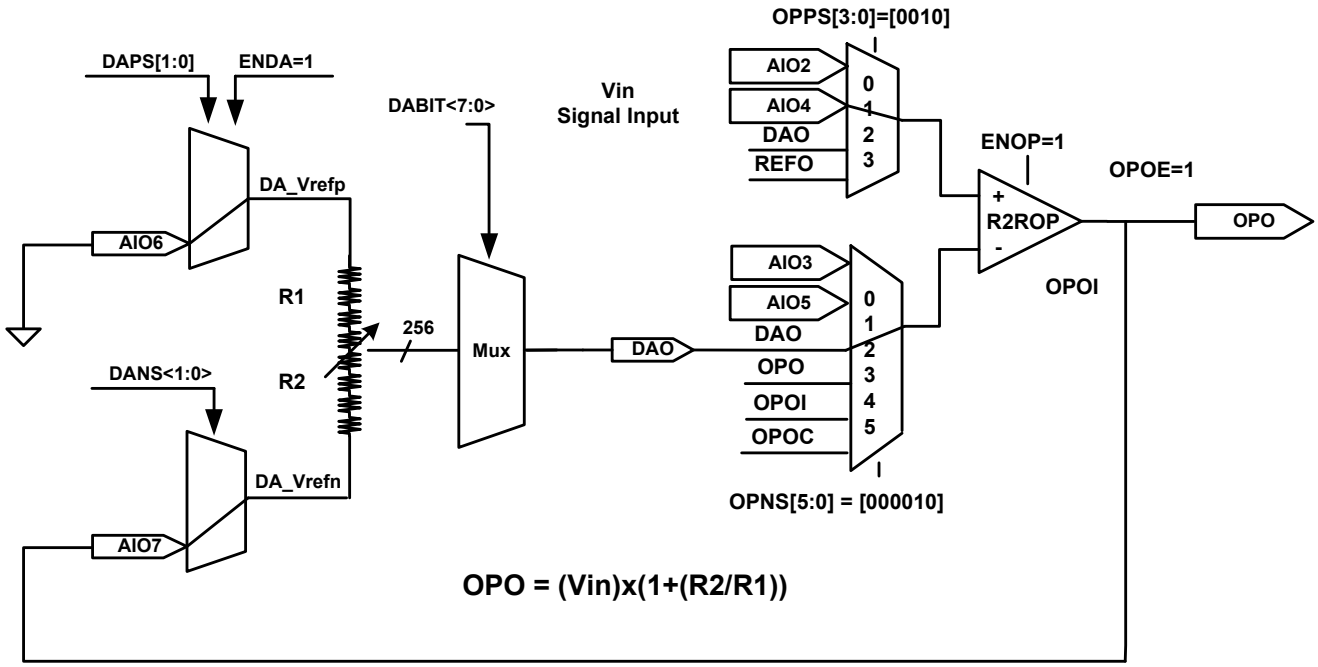
24.7. DAC application circuit I

Use DAO Output



24.8. DAC application circuit II

Use as Programmable Gain Amplifier



25. MULTIPLE FUNCTION COMPARATOR CMP

25.1. Overall description

The chip has an embedded low-power, Rail-to-Rail multi-function comparator CMP for the comparing analog signals. It has the interrupt function; when the comparison result generates, the interrupt signal also generates; and it can increase the operability for users. It has different configuration settings for different applications.

Features of CMP include:

Rail-to-Rail input range
Low operating current
2us peak pulse filter
4-bit step resistor DAC with different comparison sets.
Change and discharge paths measured by touch buttons.
Interrupt signals can be generated, which belong to the interrupt vector HW3.

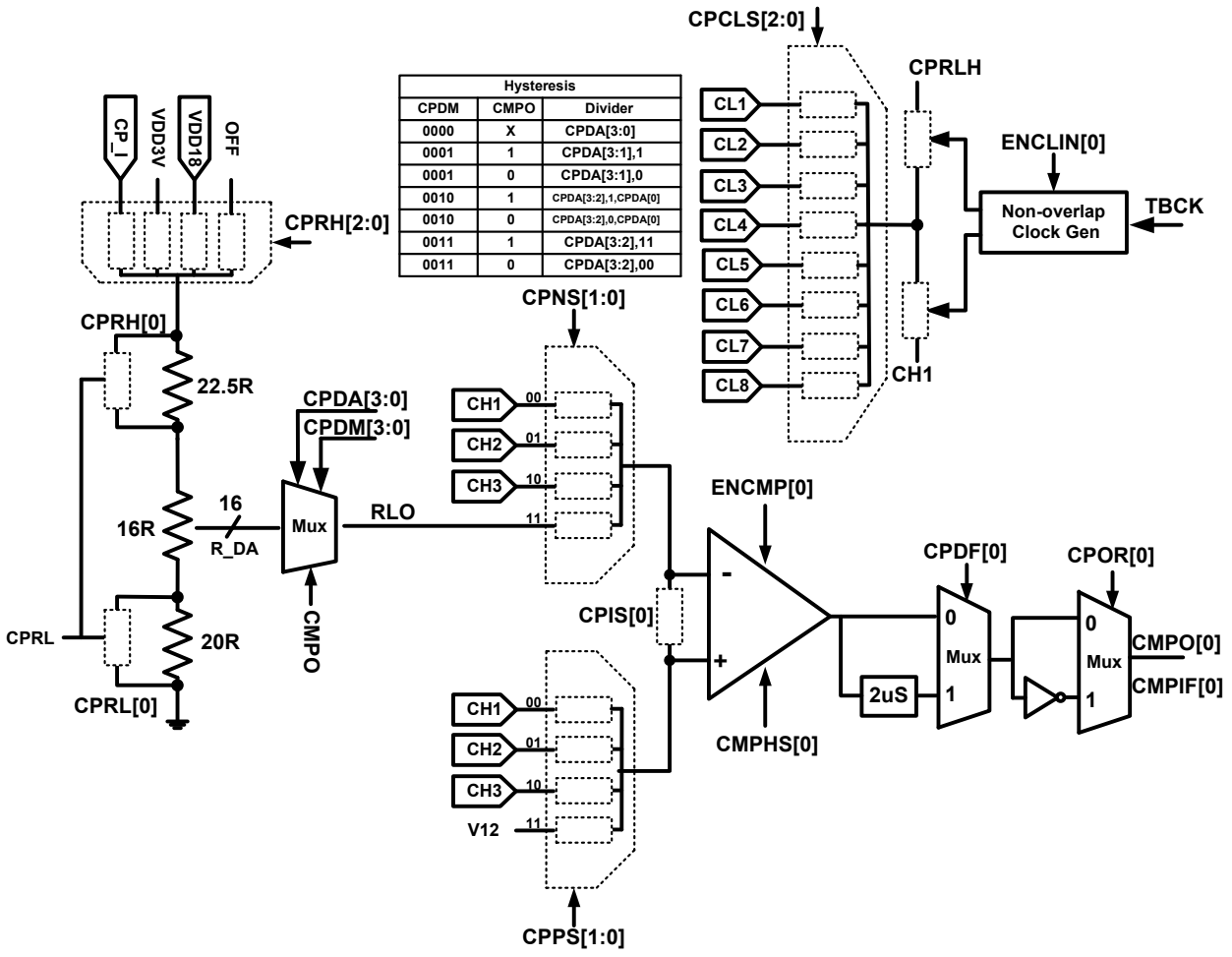


FIG. 25-1 CMP network diagram

25.1.1. Multiplexing input channel selector

The input channel of the comparator is composed two parts; one is the input channel of the comparator, which can be set by the controller CPPS[1:0]/CPNS[1:0] to respectively set the positive input channel and the negative input channel of the comparator; the other one is the touch button input channel, which can be set by the controller CPCLS[2:0]. Via proper configuration and the combination of the input channels of the two parts, the applications of the touch button can be realized. When using the comparator, the user can set the control bit CPIS as <1> to realize the short-circuit between the positive input end and the negative input end; on the contrary, if the CPIS is set as <0>, the short-circuit will not be realized.

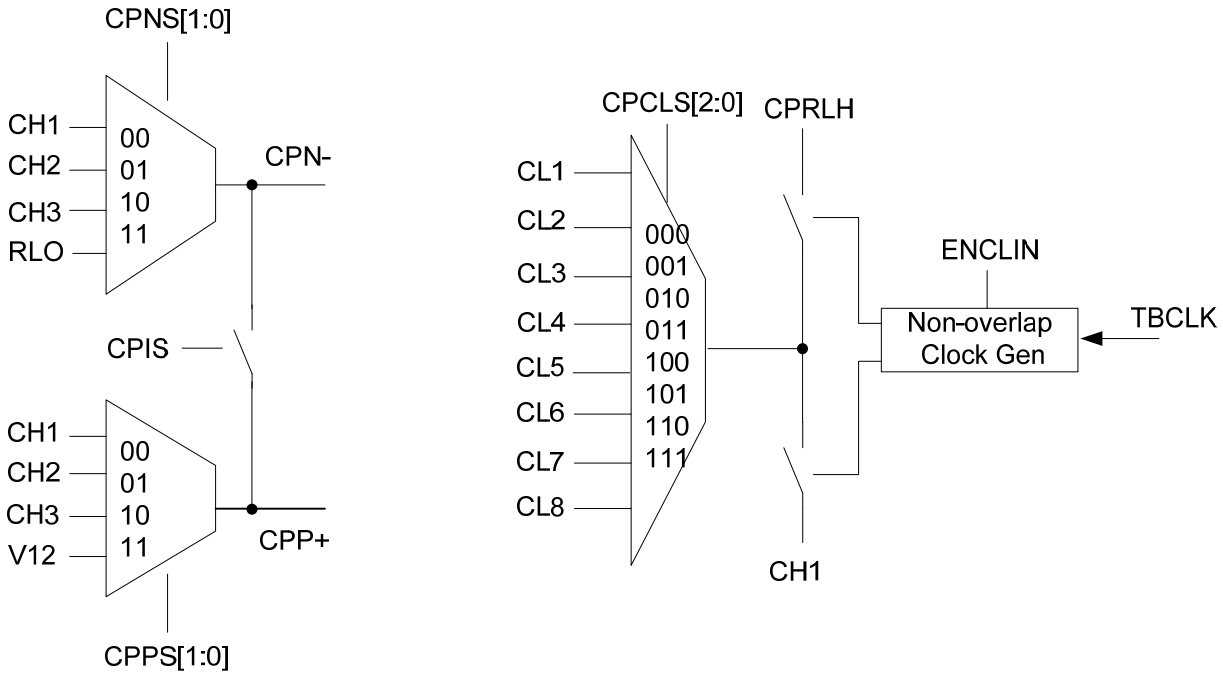


FIG. 25-2 CMP input channel framework diagram

25.1.2. Built-in multi-node resistor and resistor node selection

The comparator has a built-in multi-node resistor, and the resistor includes three parts: 22.5R, 16R and 20R. The 16R resistor is connected to a 16-stage resistor node selector; the selector divides the 16R resistor into 16 nodes, which can be set by the controllers CPDA[3:0] and CPDM[3:0] to select different resistor nodes to output different voltages to the input channel RLO of the comparator. If the control bits CPRLH and CPRLL are set as <1>, the short-circuit between the 22.5R resistor and 20R resistor can be achieved, which can adjust the resistor node voltage. The voltage sources of the multi-node resistor are VDD18/VDD3V/CP_I, and the controller CPRH[1:0] can be used to select different voltage sources to increase the output range of the node voltage.

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The hysteresis controller CPDM[3:0] is linked up with the node selector CPDA[3:0]; each bit of the hysteresis controller CPDM[3:0] is corresponding the control of the enablement and disablement of the each bit of the controller CPDA[3:0] respectively. When the corresponding bit of the hysteresis controller CPDM[3:0] is set as <1>, the hysteresis function of the corresponding bit of the node controller CPDA[3:0] will be enabled and the status of the bit is consistent with the output status of the comparator; that is CPDA[X]=CMPO. In this way, the node selector will be switched between the two nodes.

'u' means no change.

CPDM[3:0]	CMPO Output status	CPDA[3:0] Hysteresis switch period	CPDM[3:0]	CMPO Output status	CPDA[3:0] Hysteresis switch period
0000	0	uuuu	1000	0	0uuu
	1	uuuu		1	1uuu
0001	0	uuu0	1001	0	0uu0
	1	uuu1		1	1uu1
0010	0	uu0u	1010	0	0u0u
	1	uu1u		1	1u1u
0011	0	uu00	1011	0	0u00
	1	uu11		1	1u11
0100	0	u0uu	1100	0	00uu
	1	u1uu		1	11uu
0101	0	u0u0	1101	0	00u0
	1	u1u1		1	11u1
0110	0	u00u	1110	0	000u
	1	u11u		1	111u
0111	0	u000	1111	0	0000
	1	u111		1	1111

Table 25-1 Hysteresis control CPDM[3:0] configuration and values

25.1.3. Comparator output

The output of the comparator is digital output, and it will reach the IO pin PT1.7; therefore, the output of the comparator should set the IO to serve as the output mode. The output of the comparator can be set to pass through the 2us low-pass filter to eliminate the peak pulse interference. If the control bit CPDF is set as <1>, the output of the comparator will pass through the 2us low-pass filter; if the control bit CPDF is set as <0>, it will not pass through the filter. The polarity of the comparator can be set by the control bit

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CPOR. If the CPOR is set as <1>, the output of the comparator will be opposite in phase; if the CPOR is set as <0>, the output of the comparator will be normal.

25.1.4. Application of touch button

The comparator has a special function: measuring the touch button. The major principle is to set the comparison voltage via the multi-node resistor and then input which into the RLO; the multi-node resistor provides voltage to charge the touch button and then the charges of the touch button charges the external reference capacitor of the negative input channel CH1; next, the TMB counts the charge time that the voltage of the CH1 is higher than the voltage of the RLO and then determine the status that the touch button is touched or not according to the charge time.

Two switches need to be used to control the charging of the corresponding touch button and the charging of the touch button to the reference capacitor; besides, if one of the switches is close, the other one must be open. The comparator has a built-in non-overlap controller to control the switches to ensure one of them is close and the other one is open. The operating frequency of the non-overlap controller is provided by the operating clock of the TMB. Therefore, if the function should be used, it is necessary to enable the counting function of the TMB and clear the counter register of the TMB.

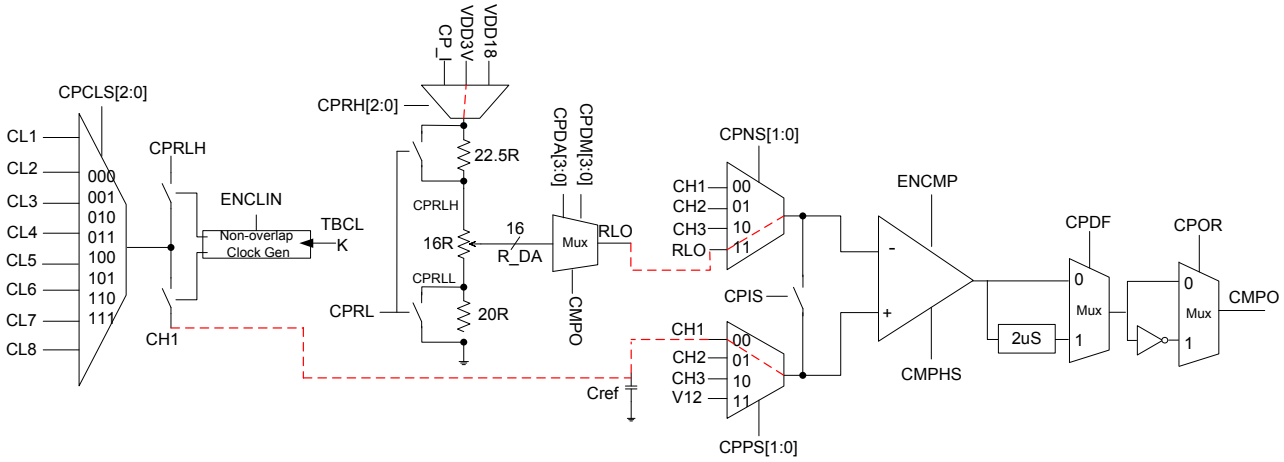

FIG. 25-4 Touch button connection diagram (One possible configuration)

25.1.5. Comparator operation initialization

The main function of the comparator is to compare the input signals; however, different modular combinations need different configurations to achieve different applications.

As a simple signal comparator:

Set the operating mode of the CMP to be low-power or normal.

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Select the input channel, including the positive input channel, negative input channel;
If the RLO is selected as the positive input channel, the reference voltage source and the voltage node of the multi-node resistor should be set;
Enable the output function of the comparator;
Set whether the output passes through the low-pass filter and the output is opposite in phase;
If the CMP comparison interrupt vector is used, the interrupt function of the comparator should be enabled;
Enable the function of the comparator.

Touch button application initialization:
Set the TMB: set the operating mode of the TMB is mode 0, set the counting-trigger source is CMPO, set the operating clock and overflow;
Set the CMP operating mode to be low-power or normal operating mode.
Select the input channel, including the positive input channel, negative input channel; the positive input channel is RLO and the negative input channel is CH1;
Set the reference voltage source and the voltage node of the multi-mode resistor; and the resistor short-circuit switch of the resistor;
Enable the output function of the comparator;
Set whether the output passes through the low-pass filter and the output is opposite in phase;
If the CMP comparison interrupt vector is used, the interrupt function of the comparator should be enabled;
Enable the function of the comparator;
Release the charges of the touch button and the reference capacitor before charging;
Disable the non-overlap controller first, and then disable the reference voltage source of the non-overlap controller, and enable the resistor short-circuit switch of the resistor;
Enable the input end short-circuit switch; discharge from the reference capacitor of the CH1to ground via the resistor;
Set the corresponding IO pin of the touch button as the output mode and the output status is 0 to discharge from the touch button to ground;
Then enable the charging function;
Disconnect the input end short-circuit switch, disconnect the resistor short-circuit of the resistor and enable the reference voltage source of the resistor;
Disable the IO output mode of the touch button;
Clear the counter register of the TMB;
Enable the non-overlap function and select the touch button to be charged;
Read the counting value of the TMb after the charging is finished.

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25.2. Register address

CMP Register Address	31 24	23 16	15 8	7 0
CMP Base Address + 0x00 (0x41800)	-	-	MASK1	REG1
CMP Base Address + 0x04 (0x41804)	MASK2	REG2	MASK3	REG3
CMP Base Address + 0x08 (0x41808)	MASK4	REG4	MASK5	REG5

-Reserved

25.3. Register function

25.3.1. CMP register 0

CMP Base Address + 0x00 (0x41800)							
Symbol	CMPCR0 (CMP Control Register 0)						
Bit	[31:17]						[16]
Name	-						CMPO
RW	-						R-0
Bit	[15:08]	[7:5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	CPIS	CPOR	CPDF	CMPHS	ENCMP
RW	R0W-0	-	RW-0				

Bit	Name	Description	
Bit[16]	CMPO	The comparison result input transferring out status of the comparator	
		0	Negative input signal > Positive input signal
		1	Positive input signal > Negative input signal
Bit[4]	CPIS	The short-circuit switch control of the comparator	
		0	Short-circuit switch opens.
		1	Short-circuit switch closes.
Bit[3]	CPOR	The digital output phase control of the comparator	
		0	Normal output
		1	Inversed output
Bit[2]	CPDF	The output low-pass filer enable control of the comparator	
		0	Disable, the output of the comparator does not pass through the 2us low-pass filter.
		1	Enable, the output of the comparator passes through the 2us low-pass filter.
Bit[1]	CMPHS	The high-speed mode enable control of the comparator	
		0	Low-power mode
		1	High-speed mode

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Bit[0]	ENCMP	Comparator function enable control	
		0	Disable (the output status is 0)
		1	Enable

25.3.2. CMP register 1

CMP Base Address + 0x04 (0x41804)					
Symbol	CMPCR1 (CMP Control Register 1)				
Bit	[31:24]	[23:20]		[19:16]	
Name	MASK	CPDM[3:0]		CPDA[3:0]	
RW	R0W-0	RW-0			
Bit	[15:08]	[7:6]	[5:4]	[3:2]	[1:0]
Name	MASK	-	CPNS	-	CPPS
RW	R0W-0	-	RW-0	-	RW-0

Bit	Name	Description	
Bit[23]	CPDM[3]	The CPDA[3] outputs hystersis enable control，and the value of the CPDA[3] is controlled by the CMPO, and keep consistent.	
		0	Disable
		1	Enable, CPDA[3]=CMPO
Bit[22]	CPDM[2]	The CPDA[2] outputs hystersis enable control，and the value of the CPDA[2] is controlled by the CMPO, and keep consistent.	
		0	Disable
		1	Enable, CPDA[2]=CMPO
Bit[21]	CPDM[1]	The CPDA[1] outputs hystersis enable control，and the value of the CPDA[1] is controlled by the CMPO, and keep consistent.	
		0	Disable
		1	Enable, CPDA[1]=CMPO
Bit[20]	CPDM[0]	The CPDA[0] outputs hystersis enable control，and the value of the CPDA[0] is controlled by the CMPO, and keep consistent.	
		0	Disable
		1	Enable, CPDA[0]=CMPO
Bit[19~16]	CPDA	Voltage division node configuration of the built-in multi-node resistor of the comparator	
		0000	0
		0001	1/16 (CPRLH – CPRLL)
		0010	2/16 (CPRLH – CPRLL)
		0011	3/16 (CPRLH – CPRLL)
		0100	4/16 (CPRLH – CPRLL)

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		0101	5/16 (CPRLH – CPRLL)
		0110	6/16 (CPRLH – CPRLL)
		0111	7/16 (CPRLH – CPRLL)
		1000	8/16 (CPRLH – CPRLL)
		1001	9/16 (CPRLH – CPRLL)
		1010	10/16 (CPRLH – CPRLL)
		1011	11/16 (CPRLH – CPRLL)
		1100	12/16 (CPRLH – CPRLL)
		1101	13/16 (CPRLH – CPRLL)
		1110	14/16 (CPRLH – CPRLL)
		1111	15/16 (CPRLH – CPRLL)
Bit[5~4]	CPNS	The negative input end selection of the comparator	
		00	CH1
		01	CH2
		10	CH3
		11	RLO
Bit[1~0]	CPPS	The positive input end selection of the comparator	
		00	CH1
		01	CH2
		10	CH3
		11	V12

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25.3.3. CMP register 2

CMP Base Address + 0x08 (0x41808)					
Symbol	CMPCR2 (CMP Control Register 2)				
Bit	[31:24]	[23:20]		[19:17]	[16]
Name	MASK	-		CPCLS	ENCLIN
RW	R0W-0			RW-0	
Bit	[15:08]	[7:5]	[4]	[3:2]	[1:0]
Name	MASK	-	CPRL	-	CPRH
RW	R0W-0	-	RW-0	-	RW-0

Bit	Name	Description	
Bit[19~17]	CPCLS	The positive input source selection of the touch button function of the comparator	
		000	CL1
		001	CL2
		010	CL3
		011	CL4
		100	CL5
		101	CL6
		110	CL7
		111	CL8
Bit[16]	ENCLIN	The built-in non-overlap function enable control of the comparator. The clock source of the non-overlap controller is TBCLK.	
		0	Disable
		1	Enable, the TBCLK is used as the driving clock source of the non-overlap controller.
Bit[4]	CPRL	The low step short-circuit switch control of the built-in step resistor of the comparator	
		0	The short-circuit switch opens, the low step resistor is not short-circuited.
		1	The short-circuit switch closes, the low step resistor is short-circuited.
Bit[2~0]	CPRH	The voltage source selection of the built-in step resistor of the comparator	
		000	Disable, no voltage supply, under high impedance
		001	CP_I , consistent with the input voltage source of the charge pump
		010	VDD3V chip operating voltage source
		100	VDD18 (1.8V voltage source from the internal LDO voltage regulator of the chip)

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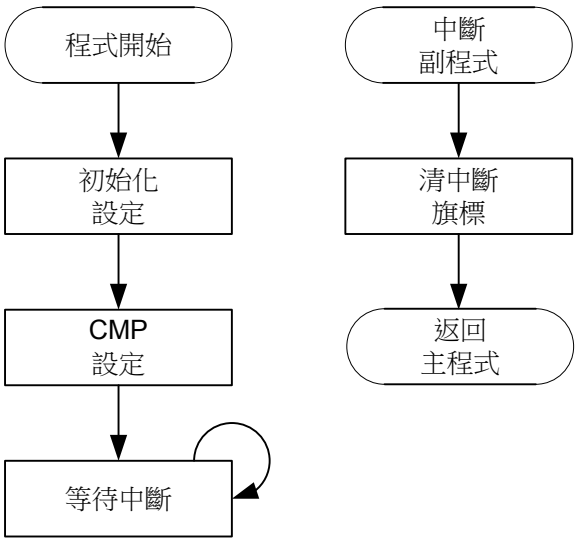
25.4. Model program flow



The program starts.
Initialization settings
CMP settings
Wait for interrupt
Interrupt the subprogram
Clear the interrupt flag
Return to the main program

25.5. Model program function

Model name: CMP usage method description

By means of proper CMP register and IO settings.
Connect the CH3(PT1.2) to the positive end of the CMP.
Connect the CH2(PT1.1) to the negative end of the CMP.
If the positive voltage of the CH3 is higher than the negative voltage of the CH2，the digital output of the CMPO is high.
If the positive voltage of the CH3 is lower than the negative voltage of the CH2，the digital output of the CMPO is low.

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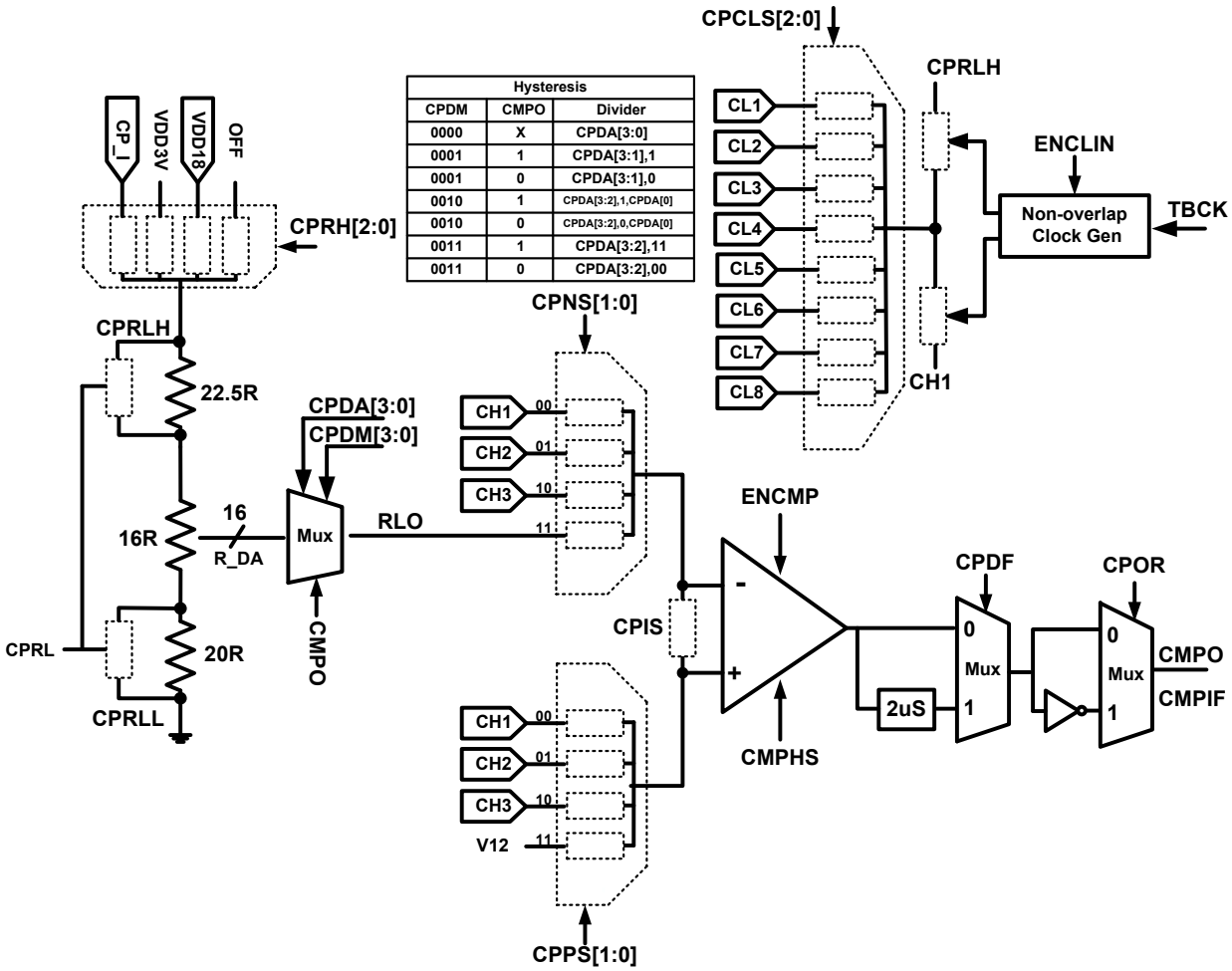


Hysteresis		
CPDM	CMPO	Divider
0000	X	CPDA[3:0]
0001	1	CPDA[3:1],1
0001	0	CPDA[3:1],0
0010	1	CPDA[3:2],1,CPDA[0]
0010	0	CPDA[3:2],0,CPDA[0]
0011	1	CPDA[3:2],11
0011	0	CPDA[3:2],00

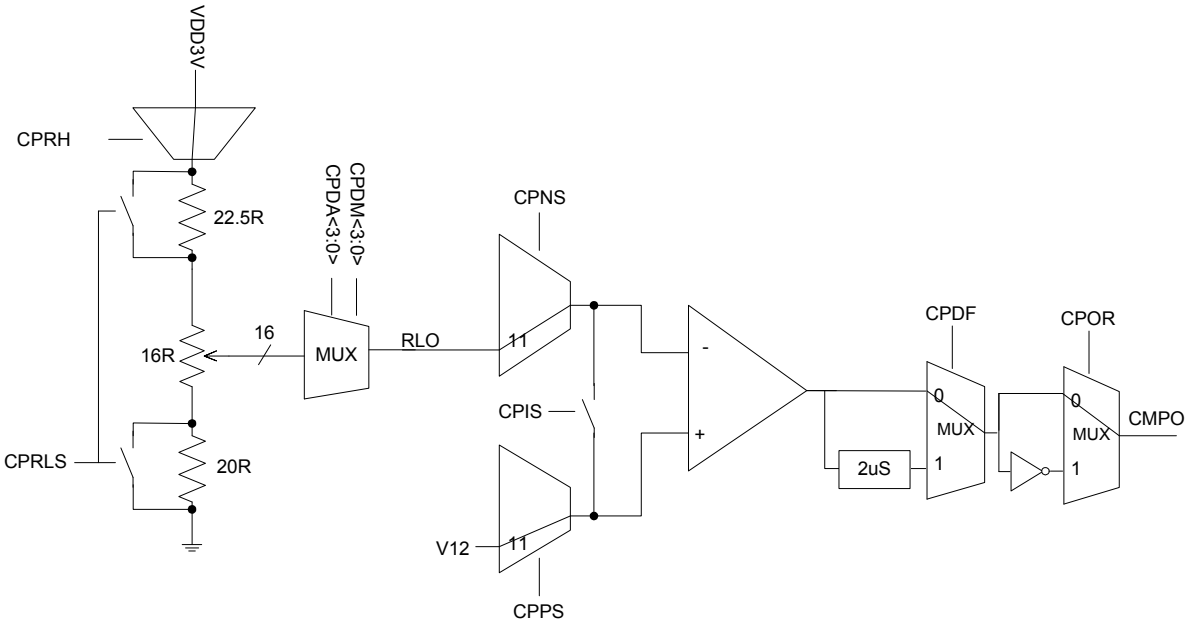
25.6. Model program description

```
00
01  #include "HY16F19X.h"
02
03  int main(void)
04  {
05      DrvGPIO_Open(E_PT1,0x80,E_IO_OUTPUT);   //PT1.7 set Output
06      DrvCMP_PInput(2);                       //CMP positive input CH3
07      DrvCMP_NInput(1);                       //CMP negative input CH2
08
09      DrvCMP_Enable();                        //CMP enable
10      DrvCMP_OutputPinEnable(0);              //Enable CMP digital output to port
11                                              //0:PT1.7
12
13
14      DrvCMP_ClearIntFlag();                  //Clear CMP interrupt flag
15      DrvCMP_EnableInt();                     //Enable CMP Interrupt
16
17
18
19      SYS_EnableGIE(7);                       //Enable GIE (Global Interrupt Enable)
20      while(1);                               //while loop
21  }
22
23  void HW3_ISR(void)
```

24	{	
25	DrvCMP_ClearIntFlag();	//Clear CMP interrupt flag
26	}	
27		

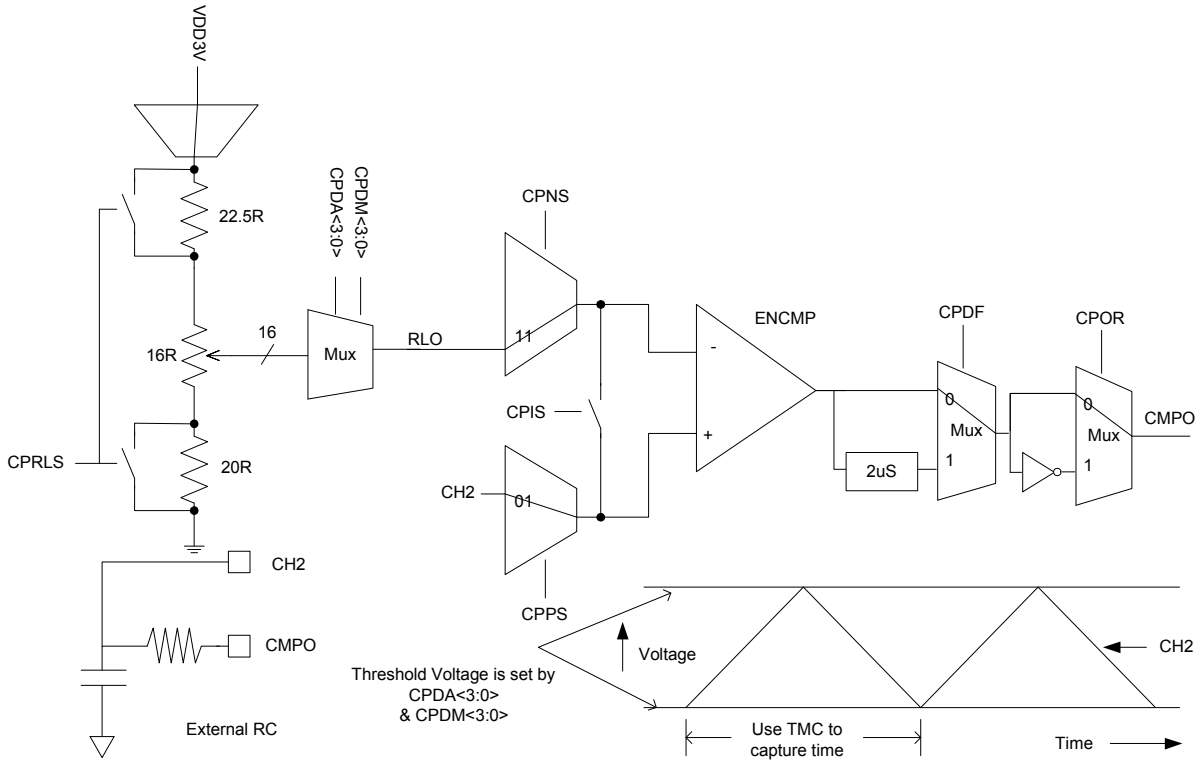
25.7. CMP application circuit I

It serves as low voltage detector.



25.8. CMP application circuit II

It is used to measure capacitors.



26. SERIAL PERIPHERAL INTERFACE (SPI)

26.1. Overall description

The HY16F19X has a serial peripheral interface (SPI).

The SPI uses the synchronous serial data communication protocol, and works under the full-duplex mode.

It communicates with the 4-wire bidirectional interface and can work under the master/slave mode.

Under the master mode, it has several configurations to execute different client devices.

Functions:

Full-duplex synchronous transmission.

Support master mode operation or slave mode operation.

Support transmitting MSB first or transmitting LSB first.

The transmission frame is 4~32-bit and can provide programmable bit length setting.

High-speed SPI bus busy-status flag.

Programmable clock pulse rate.

Support high/low potential slave end selection.

Programmable clock polarity and phase

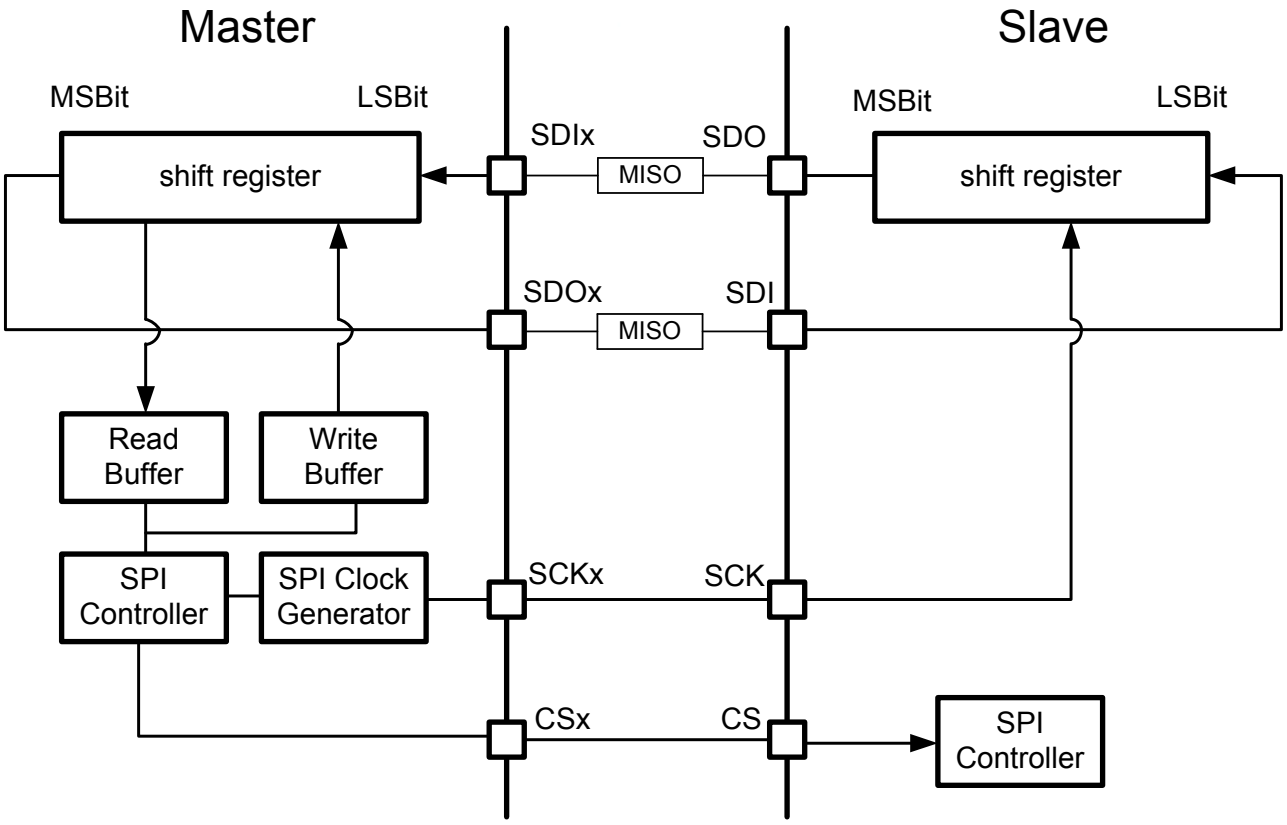


FIG. 26-1 Serial communication SPI structure diagram

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The MISO pins are the input of the master device and the output of the slave device. The MOSI pins are the output of the master device and the input of the slave device. The SCK pin is from the serial communication clock output of the master device. The CS pin is from the chip selection of the master device to enable the SPI communication of the slave device. The MOSI/MISO/SCK/CS pins of the master device or the salve device are connected together to execute tasks.

The communication is always enabled by the master device. The master device transmits data to the slave device via the MOSI pins, and the slave device replies to the master device via the MISO pins. So, that is full duplex communication; the data input and output synchronously and use the same clock source.

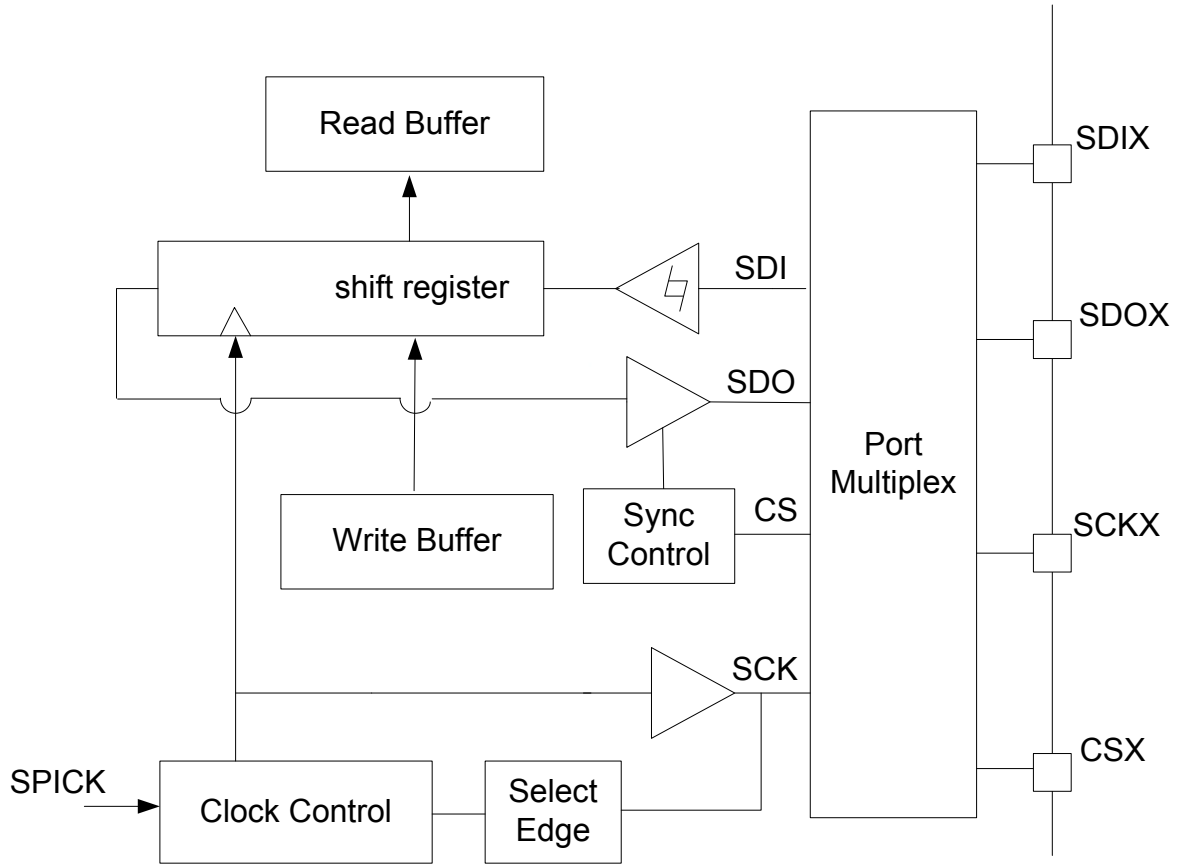

FIG. 26-2 SPI IO pin diagram

Function description: I/O pin setting:

The SPI pins can be programmed for different I/O pins.

Clock phase and clock polarity:

Four different clock types can be formed by software, and controlled by the CPOL and CPHA registers.

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The CPOL (clock polarity) is to control the stable status value of the clock without any data transmission.

It can be used in the master mode and the slave mode. If the CPOL is 1(high potential), the SCK is 1 when the SPI is under the idle mode. On the other hand, if the CPOL is 0(low potential), the SCK is 0 when the SPI is under the idle mode(low potential).

The CPHA(clock phase) controls the capturing of the data clock edge of the SCK. If the CPHA is 1(high potential), the second clock edge of the SCK pin (I the CPOL is 1, it is the falling edge; if the CPOL is 0, it is the rising edge.) will capture the data of the MSB.

The data will be locked at the second clock edge of the SCK. On the other hand, if the CPHA is 0 (low potential), the first clock edge of the SCK pin (I the CPOL is 1, it is the rising edge; if the CPOL is 0, it is the falling edge.) will capture the data of the MSB.

The data will be locked at the first clock edge of the SCK.. Therefore, the combination of the CPOL and the CPHA can control the data capturing and outputs of the clock edges.

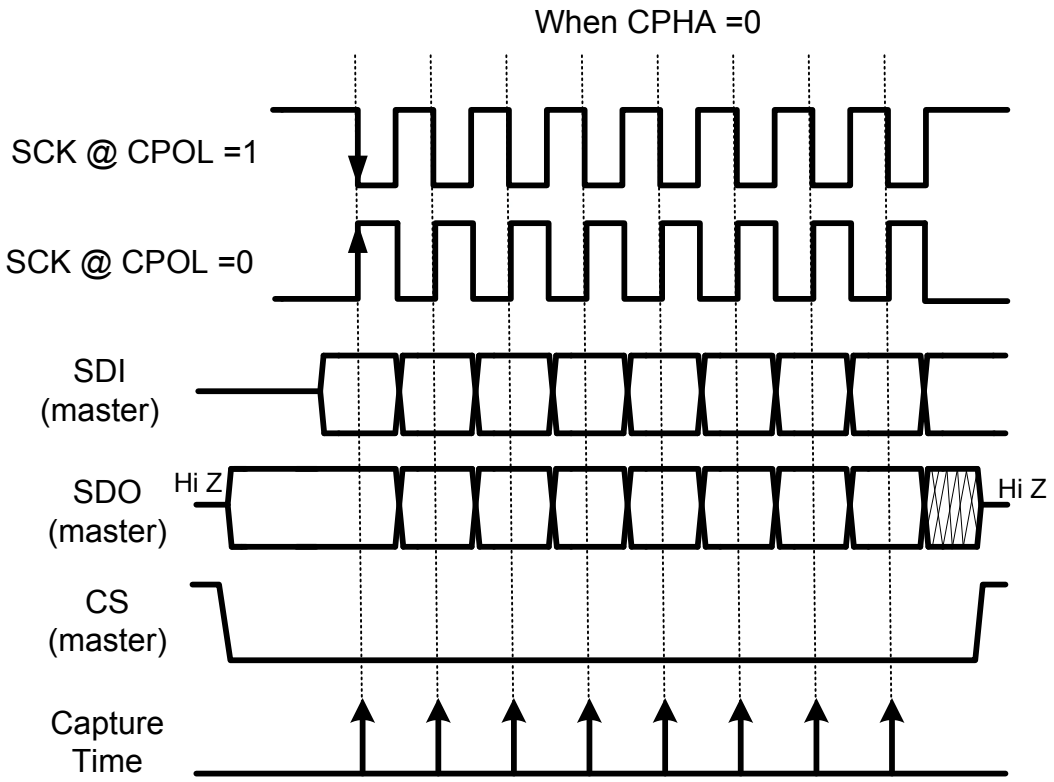

FIG. 26-3 SPI active mode clock diagram (CPHA=0)

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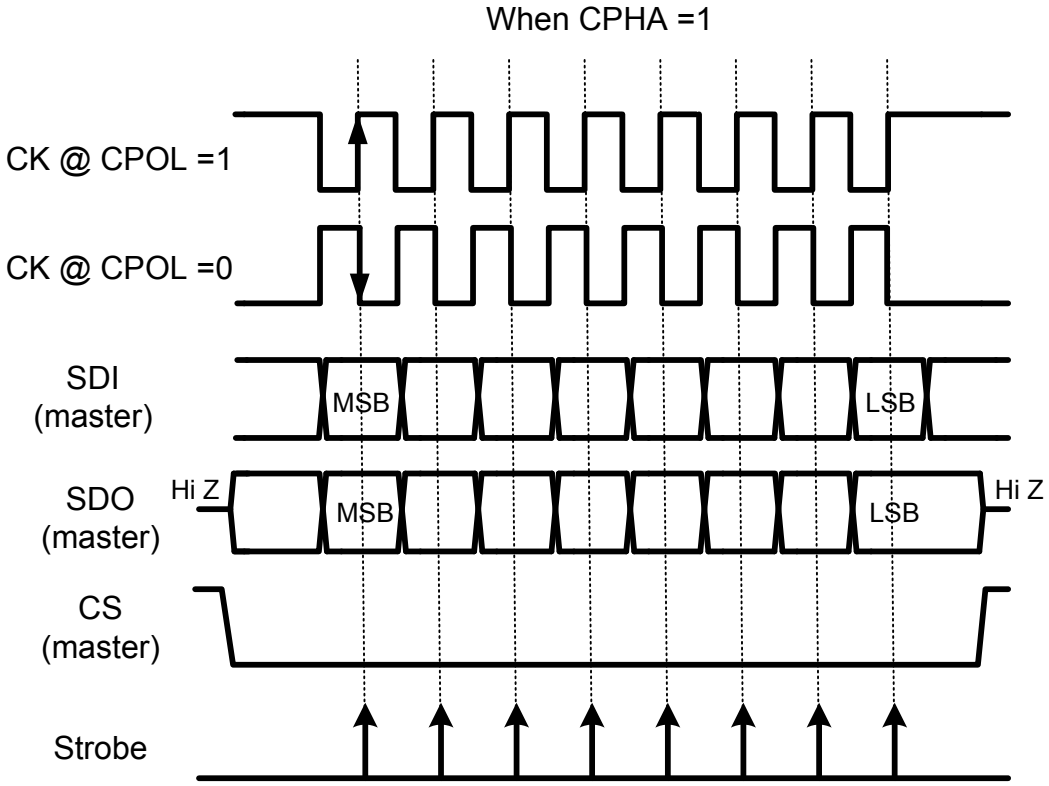

FIG. 26-4 SPI active mode clock diagram (CPHA=1)

Data frame format:

The bit length of the transaction word for transmission and reception can be defined in the SPITBL<4:0>. The lowest bit length is 4 bits, and the highest bit length is 32 bits. The transmission format of the data of the shift register can be to transmit the MSB first or transmit the LSB first, which is defined by the SPILBF. If the SPILBF is 0, the data transmission format is to transmit the MSB of the shift register first. Then, the second MSB is transmitted; finally, the LSB is transmitted. If the SPILBF is 1, the data transmission format is to transmit the LSB of the shift register first.

Select the level from the slave device chip:

The CS pin can be defined as 0 or 1 (low potential or high potential) to enable the slave device. That is controlled by the SPISCL register. If the SPISCL of the master device is 0, the CS pin will output 0 (low potential) to enable the slave device. On the other hand, if the SPISCL is 1, the CS pin will output 1 (high potential) to enable the slave device. If the SPISCL of the slave device is 0, the slave device will be enabled after receiving the input 0 (low potential) of the CS. On the other hand, if the SPISCL of the slave device is 1, the slave device will be enabled after receiving the input 1 (high potential) of the CS.

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SPIOVF:

The SPIOVF is the overflow flag of the SPI. When any additional SCK clock edge is inputted during the transmission period, it will be high potential (1). For example, if the bit length of a work is 16 bits and there are 15 clock edges from the master device before the CS is changed to high potential (in this case, the SPICSL is 0), the SPIOVF will be 1 when receiving the 17th clock edge. That means that errors occur during the transmission. If the 17th clock edge has occurred, it means that the data transmitted first are lost.

SPIABF:

The SPIABF is the interrupt flag of the SPI, which is only used in the slave mode. During the transmission, when the SCK clock edge inputs are insufficient, it will be high potential (1). For instance, if the bit length of a word is 16 bits, there are 15 clock edges from the master device and the CS is changed to high potential (in this case, the SPICSL is 0), the SPIABF is 1. That means errors occur during the transmission. The transaction is not finished and the transmitted data are updated to the read register. The transmission is stopped and lost.

SPIBUF:

The SPIBUF is the busy flag of the SPI. When the SPI is transmitting or receiving data, it is high potential (1). Under the master mode, when the SPI starts to transmit data, it is high potential (1). Once the SPI stops transmitting data or transmission is finished, it will be cleared automatically. Under the slave mode, when the SPI is ready to communicate with the master device, it is 1. Once the SPI stops transmitting data or transmission is finished, it will be cleared automatically.

Flag:

(1)SPITIF: the flag SPITIF is the transmission interrupt of the PI. When the write-in register is loaded into the shift register, it is set as 1.

(2)SPIRIF: the SPIRIF is the reception interrupt of the SPI. When the shift register is loaded into the read register, it is set as 1

26.2. Register address

SPI Register Address	31 24	23 16	15 8	7 0
SPI Base Address + 0x00(0x40F00)	SPIC2M	SPIC2	SPIC1M	SPIC1
SPI Base Address + 0x04(0x40F04)	SPIC0M	SPIC0	-	BL
SPI Base Address + 0x08(0x40F08)	RXB3	RXB2	RXB1	RXB0
SPI Base Address + 0x0C(0x40F0C)	TXB3	TXB2	TXB1	TXB0

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26.3. Register function

26.3.1. SPI register 0

SPI Base Address + 0x00 (0x40F00)										
Symbol	SPICR0 (SPI Control Register 0)									
Bit	[31]	[30:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	-	MASK	-	RxF	OVF	ABF	BUF	DCF	TxBF	RxBF
RW	-	R0W-0	-	R-0	RW0-0		R-0			
Bit	[15:12]	[11:8]	[7:4]				[3]	[2]	[1]	[0]
Name		MASK	-				CPHA	CPOL	M/S	En
RW		R0W-0	-				RW-0			

Bit	Name	Description	
Bit[22]	RxF	Reception (Rx) register update flag	
		0	Normal
		1	The reception (RX) register is updated; the reception register cannot be read now.
Bit[21]	OVF	SPI bus data over-length flag	
		0	Normal
		1	The length of the received data length is higher than the set data length BL[4:0]; writing in 0 can clear the OVF flag.
Bit[20]	ABF	SPI bus data insufficient-length flag	
		0	Normal
		1	The length of the received data length is lower than the set data length BL[4:0]; writing in 0 can clear the ABF flag.
Bit[19]	BUF	SPI bus busy flag	
		0	SPI bus interface space status
		1	SPI bus interface busy status
Bit[18]	DCF	Data lost flag	
		0	Normal
		1	The reception register is full but still keeps receiving data; the old data will be lost and reading the reception register can clear the bit.
Bit[17]	TxBF	TX transmission register full flag	
		0	TX transmission register is empty and can transmit data.
		1	TX transmission register is full and keeping writing data in the register will overwrite old data.
Bit[16]	RxBF	Rx reception register full flag	
		0	RX reception register is empty.
		1	RX reception register is full (reading the reception can clear the bit.)

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Bit[3]	CPHA	Clock phase configuration for the SPI bus capturing data	
		0	Capture data at the first clock edge of the SCK.
		1	Capture data at the second clock edge of the SCK.
Bit[2]	CPOL	SPI bus operating frequency polarity control	
		0	SCK low potential is idle.
		1	SCK high potential is idle.
Bit[1]	M/S	SPI operating mode configuration	
		0	Passive mode
		1	Active mode
Bit[0]	EN	SPI function enable control	
		0	Disable
		1	Enable

26.3.2. SPI register 1

SPI Base Address + 0x04 (0x40F04)							
Symbol	SPI CR1(SPI Control Register 1)						
Bit	[31:29]	[28:24]	[23:21]	[20]	[19]	[18]	[17:16]
Name	-	MASK	-	CSO	CSL	LBF	MD
RW	-	R0W-0	-	RW-0			
Bit	[15:5]		[4:0]				
Name	-		BL				
RW	-		RW-0				

Bit	Name	Description	
Bit[20]	CSO	Chip internal wake-up (CS) signal simulator control, applicable to the 3-wire mode	
		0	CS signal simulator works.
		1	CS signal simulator stands by.
Bit[19]	CSL	CS signal polarity configuration, for enabling devices.	
		0	Low-potential enablement
		1	High-potential enablement
Bit[18]	LBF	Data transmission order	
		0	Transmit MSB first
		1	Transmit LSB first
Bit[17-16]	MD	SPI interface operating mode configuration	
		00	SPI standard 4-wire communication interface mode
		01	SPI universal 3-wire interface mode
		10	TI mode

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		11	TI mode
Bit[4~0]	SPIBL	SPI signal word length transmission configuration	
		00000	8 bits length
		00001	16 bits length
		00010	24 bits length
		00011	4 bits length
		00100	5 bits length
		00101	6 bits length
		00110	7 bits length
		00111	8 bits length
		01000	9 bits length
		01001	10 bits length
		01010	11 bits length
		01011	12 bits length
		01100	13 bits length
		01101	14 bits length
		01110	15 bits length
		01111	16 bits length
		10000	17 bits length
		10001	18 bits length
		10010	19 bits length
		10011	20 bits length
		10100	21 bits length
		10101	22 bits length
		10110	23 bits length
		10111	24 bits length
		11000	27 bits length
		11001	26 bits length
		11010	27 bits length
		11011	28 bits length
		11100	29 bits length
		11101	30 bits length
		11110	31 bits length
		11111	32 bits length

When the MD is set as the 3-wire mode, the original CS pin will become the GPIO mode. You can use the random wave type to generate the desired signal or used in other

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applications, but you still need to use the CS SPIC interface as the synchronous signal.

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The 3-wire mode under the master mode:
No any special treatment for the internal synchronous circuit.
The 3-wire mode under the slave mode:
It needs to use the CS signal of the CSO bit analog SPI bus, use the CSO CS signal to simulate and should be similar to the standard 4-wire mode.

26.3.3. SPI register 2

SPI Base Address + 0x08 (0x40F08)	
Symbol	SPICR2 (SPI Control Register2)
Bit	[31:16]
Name	RXB31-16
RW	R-X
Bit	[15:0]
Name	RXB15-0
RW	RW-X

Bit	Name	Description
Bit[31~0]	SPIRB	SPIRB[31:0] is the 32-bit reception register.

Use the LBF bit to set whether the LSB or MSB is transmitted first.
If the LSB is set to be transmitted first, the position where the data are stored will be influenced, and the RXB effective data will be right-justified.
For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the RXB [7:0]; if the BL is set to be under the 9-bit mode, the received data will be stored at the RXB [8:0], and so on.
If the MSB is set to be transmitted first, the RXB effective data will be left-justified.
For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the RXB [31:24]; if the BL is set to be under the 9-bit mode, the received data will be stored at the RXB [31:23], and so on.

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26.3.4. SPI register 3

SPI Base Address + 0x0C (0x40F0C)	
Symbol	SPICR3 (SPI Control Register 3)
Bit	[31:16]
Name	TXB31-16
RW	R-X
Bit	[15:0]
Name	TXB15-0
RW	RW-X

Bit	Name	Description
Bit[31~0]	SPITB	SPITB[31:0] is the 32-bit transmission register.

Use the LBF bit to set whether the LSB or MSB is transmitted first.

If the LSB is set to be transmitted first, the position where the data are stored will be influenced, and the TXB effective data will be right-justified.

For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the TXB [7:0]; if the BL is set to be under the 9-bit mode, the received data will be stored at the TXB [8:0], and so on.

If the MSB is set to be transmitted first, the TXB effective data will be left-justified.

For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the TXB [31:24]; if the BL is set to be under the 9-bit mode, the received data will be stored at the TXB [31:23], and so on.

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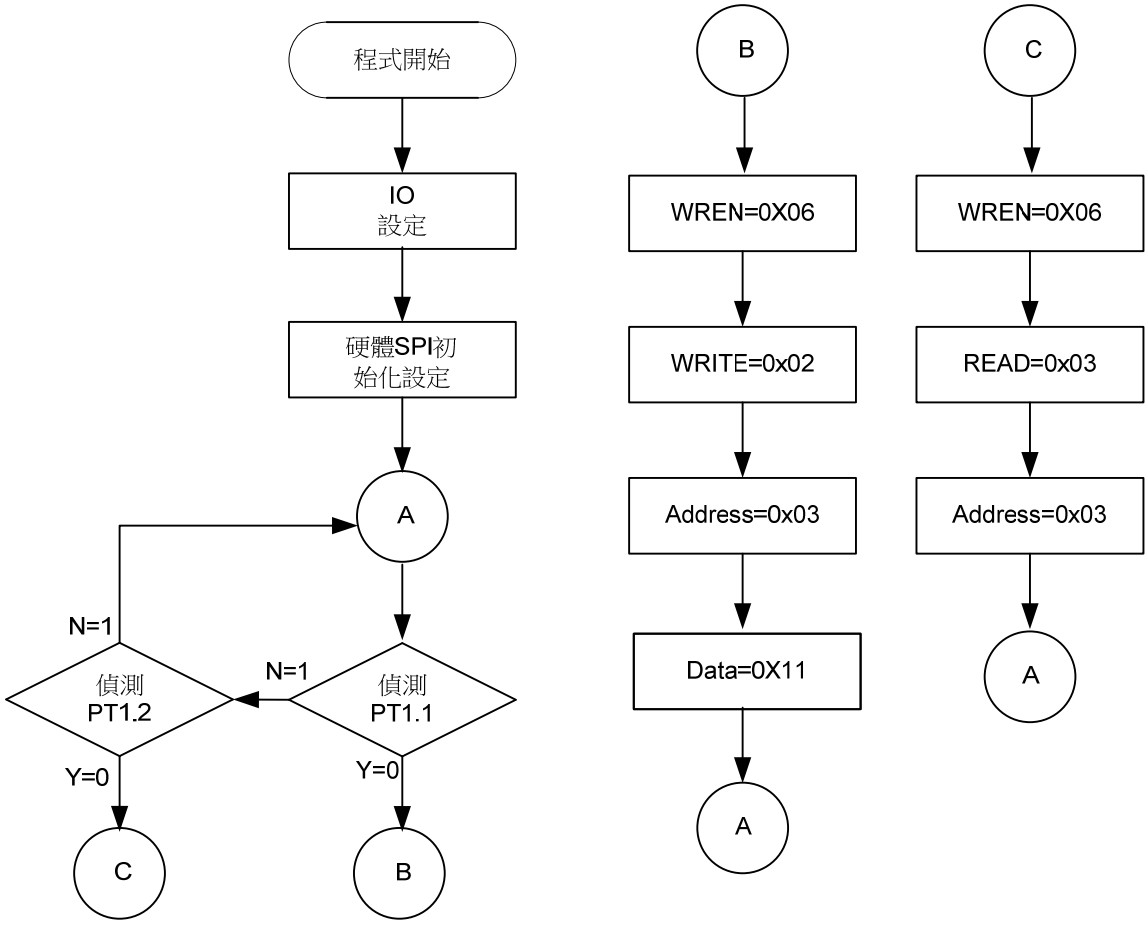
26.4. Model program flow



The program starts.

IO settings

Hardware SPI initialization settings

Detect

Detect

26.5. Model program function

Model name: communication SPI interrupt settings

The setting can be done via the SPI pins and the SPI register.

Test the write-in function of the hardware SPI to the AT93C46.

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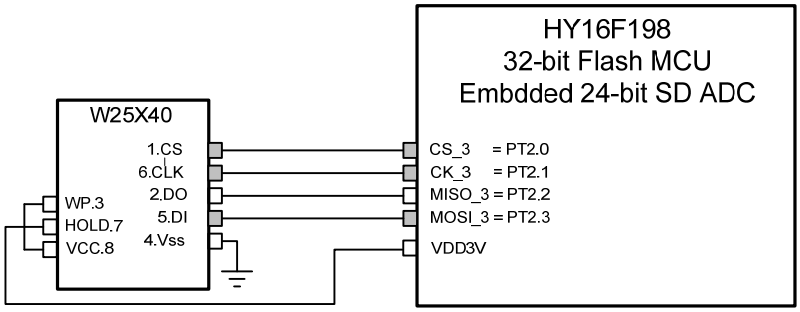
HY16F198
32-bit Flash MCU
Embdded 24-bit SD ADC
W25X40
1.CS
6.CLK
2.DO
5.DI
4.Vss
WP.3
HOLD.7
VCC.8
CS_3 = PT2.0
CK_3 = PT2.1
MISO_3 = PT2.2
MOSI_3 = PT2.3
VDD3V

26.6. Model program description

(Main program)

```
0
1  #include "HY16F19X.h"
2
3
4  volatile unsigned int i,a;
5
6  void InitalSPI32(void);
7  void Delay(unsigned int num);
8
9  int main(void)
10 {
11    SPI32_INI();
12    DrvGPIO_Open(E_PT1,0x06,E_IO_INPUT);          //PT1 BIT3~0 pull high
13    DrvGPIO_Open(E_PT1,0xf6,E_IO_PullHigh );
14
15 while(1)
16    {
17       DrvGPIO_SetBit(E_PT2,0);                   //PT2.0 CS=1
18       i=DrvGPIO_GetBit(E_PT1,1);                 //read PT1.1 pin high or low
19       while(i==0)
20       {
21          i=1;
22
23          DrvGPIO_ClrBit(E_PT2,0);                //PT2.0 CS=1
24          DrvSPI32_Write(0x06000000);             //CMD=0x06 =>Write.Read enable
25          spi_busy=1;
26          while(spi_busy){spi_busy=(spi_00>>19)&0x01;}
27          DrvGPIO_SetBit(E_PT2,0);                //PT2.0 CS=0
28          Delay(0x20);
29
30
31          DrvGPIO_ClrBit(E_PT2,0);                //PT2.0 CS=1
32          DrvSPI32_Write(0x02000000);             //CMD=0x02 =>Write EN
33          spi_busy=1;
34          while(spi_busy){spi_busy=(spi_00>>19)&0x01;}
35
36          DrvSPI32_BitLength(24);
37          DrvSPI32_Write(0x000300);               //Address 0x03
38          spi_busy=1;
39          while(spi_busy){spi_busy=(spi_00>>19)&0x01;}
40
41          DrvSPI32_BitLength(8);
42          DrvSPI32_Write(0x11000000);             //Data 0x11
43          spi_busy=1;
44          while(spi_busy){spi_busy=(spi_00>>19)&0x01;}
45
46
47          DrvGPIO_SetBit(E_PT2,0);//PT2.0 CS=0
48          Delay(0x20);
49       }
50       Delay(0x200);
51
52       DrvGPIO_SetBit(E_PT2,0);//PT2.0 CS=1
53       i=DrvGPIO_GetBit(E_PT1,2);                 //read PT1.2 pin high or low
```

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```
54      while(i==0)
55      {
56       i=1;
57            DrvGPIO_ClrBit(E_PT2,0)                ;//PT2.0 CS=1
58            DrvSPI32_Write(0x06000000);            //CMD=0x06 =>Write.Read enable
59            spi_busy=1;
60            while(spi_busy){spi_busy=(spi_00>>19)&0x01;}
61            DrvGPIO_SetBit(E_PT2,0);               //PT2.0 CS=0
62            Delay(0x20);
63
64            DrvGPIO_ClrBit(E_PT2,0);               //PT2.0 CS=1
65            DrvSPI32_Write(0x03000000);            //CMD=0x02 =>Read EN
66            spi_busy=1;
67            while(spi_busy){spi_busy=(spi_00>>19) & 0x01;}
68
69            DrvSPI32_BitLength(24);
70            DrvSPI32_Write(0x000300);              //Address 0x03
71            spi_busy=1;
72            while(spi_busy){spi_busy=(spi_00>>19) & 0x01;}
73
74            DrvSPI32_BitLength(8);
75            DrvSPI32_Write(0x55000000);
76            spi_busy=1;
77            while(spi_busy){spi_busy=(spi_00>>19) & 0x01;}
78            temp=(spi_08 >> 24 )& 0xff;
79
80            DrvGPIO_SetBit(E_PT2,0);               //PT2.0 CS=0
81            Delay(0x20);
82      }
83
84   }
85
86   asm("NOP");
87 }
```

(Subprogram)

```
0
1   void HW0_ISR(void)
2   {
3      DrvSPI32_ClrIntTxFlag();
4      temp=DrvSPI32_Read();
5   }
6
7   void InitalSPI32(void)
8   {
9      asm("NOP");
10     //Set SPI input pin                                  //Master2,3-wire mode
11     DrvGPIO_Open(E_PT2,0x0b,E_IO_OUTPUT);//CS=PT2.0 output //CPHA=0 CPOL=1
12     DrvGPIO_Open(E_PT2,0x04,E_IO_INPUT);//               //Port2.0 =CS
13                                                         // Port2.1 =CK
14                                                         // Port2.2 = DI
15                                                         // Port2.3 =DO
16     DrvGPIO_SetPortBits(E_PT2,0x01);                    //SPI GPIO
17
18     DrvSPI32_Open(E_DRVSPI_MASTER2,E_DRVSPI_TYPE0,2,4);
19     DrvSPI32_Enable();
```

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20	asm("NOP");	
21	}	
22		
23		
24	void Delay(unsigned int num)	//Software Delay Subroutines
25	{	
26	volatile unsigned int d;	
27	for(d=0;d<=num;d++);asm("NOP");	
28	}	
29		
30		

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27. ENHANCED UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMIT (EUART)

27.1. Overall description

The chip has an embedded enhanced universal asynchronous receiver transmit (EUART) management. The peripheral devices of the EUART is so called serial communication interface (SCI). The EUART can be set as the full-duplex asynchronous system, and its peripheral communication devices, including ADC or DAC integrated circuit, serial EEPROM/Flash, etc. The EUART has extra features, including the data frame error detection and automatic address identification. The data frame error detection can determine whether a data frame is valid or passes the frame stop bit. The automatic address identification can compare the address frame content with the single chip address; and the serial interrupt can only be generated when both of them are conformed to each other.

27.1.1. Communication IO pins

The EUART communication bus only uses two wires, TX/RX; the chip allocates 8 sets of communication IO pins (each set includes the TX/RX wires) for the EUART module for users to perform designs freely. However, the reuse functions of the IO port can be used to conveniently select and enable the communication IO pins of the EUART via the controller PTUR[2:0]/PTURE; accordingly, when using the EUART, the IO communication pins should be enabled, and the corresponding IO pins should be set as the input mode or output mode. The distribution of the EUART communication IO pins is as shown in the following table.

UART

PTUR[2:0]	PTURE	TX	RX	PTUR[2:0]	PTURE	TX	RX
000	1	PT1.0	PT1.1	100	1	PT8.0	PT8.1
001	1	PT1.4	PT1.5	101	1	PT8.4	PT8.5
010	1	PT2.0	PT2.1	110	1	PT9.0	PT9.1
011	1	PT2.4	PT2.5	111	1	PT9.4	PT9.5

UART2

PTUR2[2:0]	PTURE	TX2	RX2	PTUR2[2:0]	PTURE	TX2	RX2
000	1	PT1.2	PT1.3	100	1	PT8.2	PT8.3
001	1	PT1.6	PT1.7	101	1	PT8.6	PT8.7
010	1	PT2.2	PT2.3	110	1	PT9.2	PT9.3
011	1	PT2.6	PT2.7	111	1	PT9.6	PT9.7

Table 22-1 EUART communication IO pin distribution

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27.2. Register address

UART Register Address	31	24	23	16	15	8	7	0
UART Base Address + 0x00(0x40E00)	Mask0		REG0		Mask1		REG1	
UART Base Address + 0x04(0x40E04)	-		-		Mask2		REG2	
UART Base Address + 0x08(0x40E08)	-		-		Baud Rate			
UART Base Address + 0x0C(0x40E0C)	-		Tx		-		Rx	

-Reserved

27.3. Register function

27.3.1. UART register 0

UART Base Address + 0x00 (0x40E00)									
Symbol	UARTCR0 (UART Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	Mask	OErr	NErr	FErr	PErr	TxBusy	TxBF	RxBusy	RxBF
RW	R0W-0	RW0-0				R-0			
Bit	[15:08]	[7:6]		[5:4]		[3]	[2]	[1]	[0]
Name	MASK	PLen		DLen		RxIT	RxEn	TxIT	TxEn
RW	R0W-0	RW-1		RW-2		RW-0			

Bit	Name	Description	
Bit[23]	OErr	Rx Buffer over run error flag	
		0	Normal
		1	Over run
Bit[22]	OErr	Rx Noise detected flag	
		0	Normal
		1	Noise detected
Bit[21]	FErr	Rx Frame check error flag	
		0	Normal
		1	Frame check error
Bit[20]	PErr	Rx Parity check error	
		0	Normal
		1	Parity check error
Bit[19]	TxBusy	Tx Busy flag	
		0	Idle
		1	Busy
Bit[18]	TxBF	Tx Buffer Full flag	
		0	Empty
		1	Full

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Bit[17]	RxBusy	Rx Busy flag		
		0	Idle	
		1	Busy	
Bit[16]	RxBF	Rx Buffer Full flag		
		0	Empty	
		1	Full	
Bit[7~6]	PLen	Tx stop length control		
		0	0.5Bit	
		1	1Bit	
		2	1.5Bit	
		3	2 Bit	
Bit[5~4]	PLen	Tx/Rx data length		
			Normal Mode	Parity Check Mode
		0	6 Bit Mode	5 Bit Mode
		1	7 Bit Mode	6 Bit Mode
		2	8 Bit Mode	7 Bit Mode
		3	9 Bit Mode	8 Bit Mode
Bit[3]	RxIT	Rx interrupt method selection		
		0	Send out the interrupt when the Rx Data Buffer has data, and the interrupt disappears after the data are read.	
		1	Send out the interrupt after one piece of data is received by the Rx.	
Bit[2]	RxEn	UART Rx control switch		
		0	Disable	
		1	Enable	
Bit[1]	TxIT	Tx interrupt method selection		
		0	Send out the interrupt when the Tx Data Buffer is idle, and the interrupt disappears after the data are written in.	
		1	Sent out the interrupt after one piece of data is transmitted by the Tx.	
Bit[0]	TxEn	UART Tx control switch		
		0	Disable	
		1	Enable	

23.3.2 UART register 1

UART Base Address + 0x04 (0x40E04)	
Symbol	UARTCR1 (UART Control Register 1)
Bit	[31:16]
Name	RSV.
RW	R-0

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Bit	[15:08]	[7:5]	[4]	[3]	[2]	[1]	[0]
Name	Mask	-	RxABDF	RxABDEn	RxWUEn	PrtEn	PrtODD
RW	R0W-0	-	RW-0				

Bit	Name	Description	
Bit[4]	RxABDF	Automatic baud rate detection switch	
		0	Disable
		1	Enable
Bit[3]	RxABDEn	Automatic baud rate detection error flag	
		0	Normal
		1	Error occurs
Bit[2]	RxWUEn	Automatic wake-up mode	
		0	Disable
		1	Enable
Bit[1]	PrtEn	Parity check switch	
		0	Disable
		1	Enable
Bit[0]	PrtODD	Select the odd parity check, even parity check	
		0	Even parity check
		1	Odd parity check

27.3.2. UART register 2

UART Base Address + 0x08 (0x40E08)	
Symbol	UARTCR2 (UART Control Register 2)
Bit	[31:16]
Name	RSV.
RW	R-0
Bit	[15:0]
Name	Baud Rate
RW	RW-X

Bit	Name	Description
Bit[15~0]	Baud Rate	UART baud rate setting

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27.3.3. UART register 3

UART Base Address + 0x0C (0x40E0C)		
Symbol	UARTCR3 (UART Control Register 3)	
Bit	[31:27]	[24:16]
Name	-	Tx Data
RW	-	W-X
Bit	[15:8]	[7:0]
Name	-	Rx Data
RW	-	R-X

Bit	Name	Description
Bit[24~16]	Tx Data	Tx Data Buffer
Bit[7~0]	Rx Data	Rx Data Buffer

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28. ENHANCED UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMIT (EUART2)

28.1. Register address

UART2 Register Address	31	24	23	16	15	8	7	0
UART2 Base Address + 0x00(0x40E10)	Mask0		REG0		Mask1		REG1	
UART2 Base Address + 0x04(0x40E14)	-		-		Mask2		REG2	
UART2 Base Address + 0x08(0x40E18)	-		-		Baud Rate			
UART2 Base Address + 0x0C(0x40E1C)	-		Tx		-		Rx	

-Reserved

28.2. Register function

28.2.1. UART2 register 0

UART2 Base Address + 0x10 (0x40E10)									
Symbol	UART2CR0 (UART2 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	Mask	OErr	NErr	FErr	PErr	TxBusy	TxBF	RxBusy	RxBF
RW	R0W-0	RW0-0				R-0			
Bit	[15:08]	[7:6]		[5:4]		[3]	[2]	[1]	[0]
Name	MASK	PLen		DLen		RxIT	RxEn	TxIT	TxEn
RW	R0W-0	RW-1		RW-2		RW-0			

Bit	Name	Description	
Bit[23]	OErr	Rx Buffer over run error flag	
		0	Normal
		1	Over run
Bit[22]	OErr	Rx Noise detected flag	
		0	Normal
		1	Noise detected
Bit[21]	FErr	Rx Frame check error flag	
		0	Normal
		1	Frame check error
Bit[20]	PErr	Rx Parity check error	
		0	Normal
		1	Parity check error
Bit[19]	TxBusy	Tx Busy flag	
		0	Idle
		1	Busy

Bit[18]	TxBF	Tx Buffer Full flag		
		0	Empty	
		1	Full	
Bit[17]	RxBusy	Rx Busy flag		
		0	Idle	
		1	Busy	
Bit[16]	RxBF	Rx Buffer Full flag		
		0	Empty	
		1	Full	
Bit[7~6]	PLen	Tx stop length control		
		0	0.5Bit	
		1	1Bit	
		2	1.5Bit	
		3	2 Bit	
Bit[5~4]	PLen	Tx/Rx data length		
			Normal Mode	Parity Check Mode
		0	6 Bit Mode	5 Bit Mode
		1	7 Bit Mode	6 Bit Mode
		2	8 Bit Mode	7 Bit Mode
		3	9 Bit Mode	8 Bit Mode
Bit[3]	RxIT	Rx interrupt method selection		
		0	Send out the interrupt when the Rx Data Buffer has data, and the interrupt disappears after the data are read.	
		1	Send out the interrupt after one piece of data is received by the Rx.	
Bit[2]	RxEn	UART Rx control switch		
		0	Disable	
		1	Enable	
Bit[1]	TxIT	Tx interrupt method selection		
		0	Send out the interrupt when the Tx Data Buffer is idle, and the interrupt disappears after the data are written in.	
		1	Sent out the interrupt after one piece of data is transmitted by the Tx.	
Bit[0]	TxEn	UART Tx control switch		
		0	Disable	
		1	Enable	

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28.2.2. UART2 register 1

UART2 Base Address + 0x14 (0x40E14)							
Symbol	UART2CR1 (UART2 Control Register 1)						
Bit	[31:16]						
Name	RSV.						
RW	R-0						
Bit	[15:08]	[7:5]	[4]	[3]	[2]	[1]	[0]
Name	Mask	-	RxABDF	RxABDEn	RxWUEn	PrtEn	PrtODD
RW	R0W-0	-	RW-0				

Bit	Name	Description	
Bit[4]	RxABDF	Automatic baud rate detection switch	
		0	Disable
		1	Enable
Bit[3]	RxABDEn	Automatic baud rate detection error flag	
		0	Normal
		1	Error occurs
Bit[2]	RxWUEn	Automatic wake-up mode	
		0	Disable
		1	Enable
Bit[1]	PrtEn	Parity check switch	
		0	Disable
		1	Enable
Bit[0]	PrtODD	Select the odd parity check, even parity check	
		0	Even parity check
		1	Odd parity check

28.2.3. UART2 register 2

UART2 Base Address + 0x18 (0x40E18)	
Symbol	UART2CR2 (UART2 Control Register 2)
Bit	[31:16]
Name	RSV.
RW	R-0
Bit	[15:0]
Name	Baud Rate
RW	RW-X

Bit	Name	Description
Bit[15~0]	Baud Rate	UART baud rate setting

28.2.4. UART2 register 3

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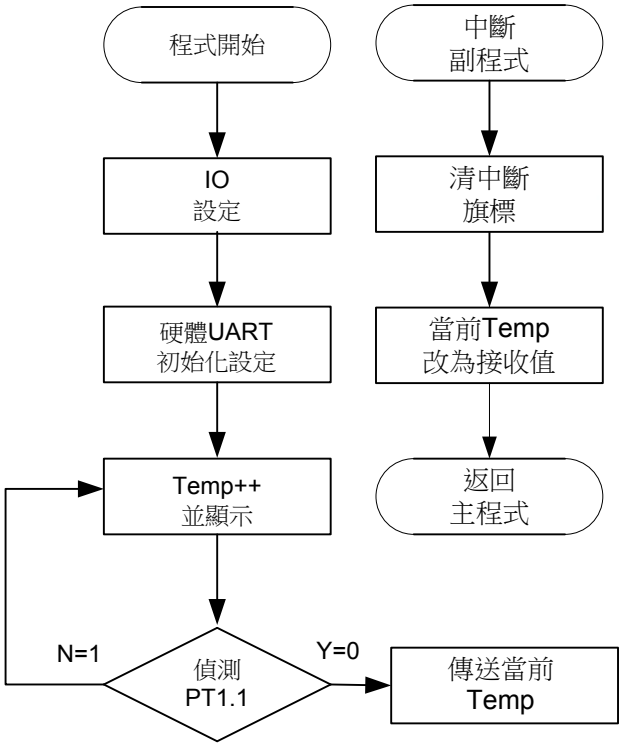
UART2 Base Address + 0x1C (0x40E1C)		
Symbol	UART2CR3 (UART2 Control Register 3)	
Bit	[31:27]	[24:16]
Name	-	Tx Data
RW	-	W-X
Bit	[15:8]	[7:0]
Name	-	Rx Data
RW	-	R-X

Bit	Name	Description
Bit[24~16]	Tx Data	Tx Data Buffer
Bit[7~0]	Rx Data	Rx Data Buffer

28.3. Model program flow



The program starts.
IO setting
Hardware UART initialization settings
and display
Detect
Transmit the current Temp
Interrupt the subprogram
Clear the interrupt flag

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The current Temp is changed to be the reception value.

Return to the main program

28.4. Model program function

Model name: communication protocol EUART interrupt setting

Connect the TX and RX PIN to the RS232 related circuits.

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28.5. Model program description

Main program

```
0
1  int main(void)
2  {
3     DisplayInit();
4     ClearLCDframe();
5     InitUartPort();
6     temp = 0;
7     Buffer_Start =0;
8     DrvGPIO_Open(E_PT1,0x02,E_IO_INPUT);
9     DrvGPIO_Open(E_PT1,0x02,E_IO_PullHigh );
10
11    while(1)
12    {
13          i=DrvGPIO_GetBit(E_PT1,1);//read PT1.1 pin high or low
14          if(i==0)
15          {
16                DrvUART_EnableInt(1,1);
17                Delay(0x8000);
18          }
19          Delay(0x8000);
20          LCD_DATA_DISPLAY(temp++);
21     }
22 }
```

Subprogram

```
0
1  void InitUartPort(void)
2  {
3     DrvGPIO_Open(E_PT2,0x01,E_IO_OUTPUT);          //PT1.0 output TX_1
4     DrvGPIO_Open(E_PT2,0x02,E_IO_INPUT);           //PT1.1   input   RX_1
5     DrvCLOCK_EnableHighOSC (E_EXTERNAL,50);        //En HSXT
6     DrvUART_ClkEnable(0,0);                        //En UART Int
7     outw(0x40e00,   0xff65);                       //ur_00
8     outw(0x40e04,   0xff00);                       //ur _04
9     outw(0x40e08,   0x68);                         //Set the baud rate is
                                                     9600
10    DrvUART_ConfigIO(1,2);                         //Set the Tx Rx as the IO.
11    DrvUART_EnableInt(0,1);                        //Enable the RX interrupt
12
13    asm volatile("sethi $r0, 0xc0000");
14    asm volatile("ori   $r0, $r0, 0x003f");
15    asm volatile("mtsr $r0, $INT_MASK");
16    asm volatile("movi $r0, 0x70009");
17    asm volatile("mtsr $r0, $PSW");
18 }
19 void HW0_ISR(void)
20 {
21     int a;
22     a=(inw(0x40000) & 0x08) && (inw(0x40000) & 0x080000);   //DrvUART_GetTxFlag();
23     If(a)
24     {
25          i=temp;
26          outw(0x40e0c,   (i<<16));                  // TX set Buffer
```

27	outw(0x40000, 0x08000800);	// int_00
28	}	
29	a=(inw(0x40000) & 0x04) && (inw(0x40000) & 0x040000);	//RX interrupt
30	If(a)	
31	{	
32	temp = inw(0x40e0c) & 0xff;	// RX get Buffer
33	outw(0x40000, 0x04040400);	// int_00
34	}	
35		
36	asm volatile("sethi $r0, 0xc0000");	
37	asm volatile("ori $r0, $r0, 0x003f");	
38	asm volatile("mtsr $r0, $INT_MASK");	
39	asm volatile("movi $r0, 0x70009");	
40	asm volatile("mtsr $r0, $PSW");	
41	}	
42		

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29. I2C COMMUNICATION INTERFACE

29.1. Overall description

Communication interface (CI)

I2C serial communication major classes.

I2C serial interface (Cross integrated circuit serial interface)

I2C communication interface has two operating modes, including the master mode and the slave mode.

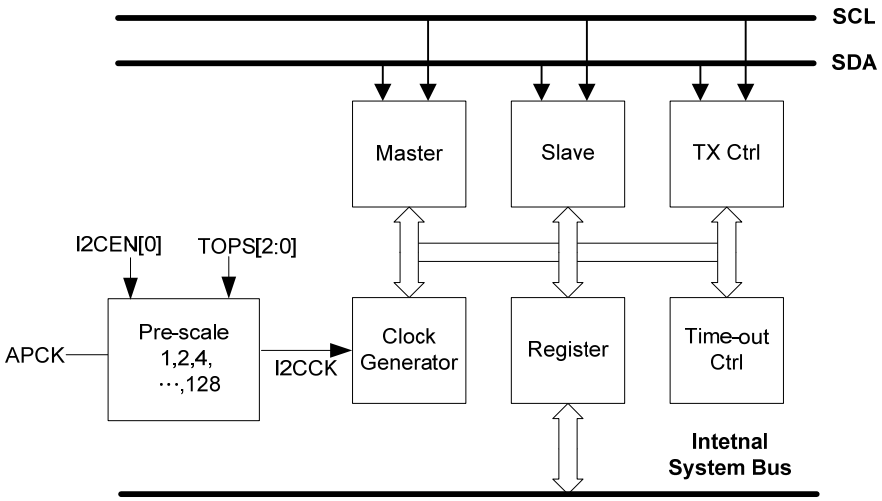

FIG. 29-1 I2C communication structure diagram

29.1.1. Communication I2C interface features:

The standard I2C serial interface includes the SDA and the SCL with two pins.

The pin has the open-type open drain output structure, which needs the external pull-up resistor to ensure the high-level output. The standard I2C serial interface is be set to be under the master mode, slave mode or the master/slave mode. The programmable clock is allowed to adjust the transmission rate of the I2C.

The data are bi-directionally transmitted between the master and the slave.

The I2C allows large operating voltage range. The reference design of the I2C uses a 7-bit length address space but reserves 16 address to deal with a group of buses and the communication between up to 112 nodes.

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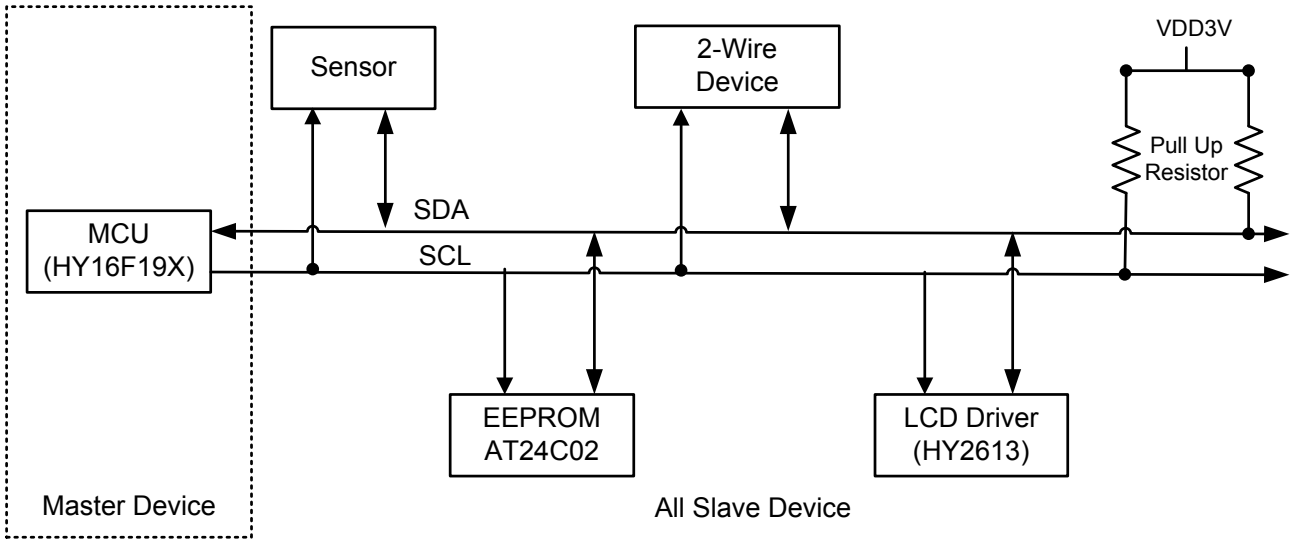

FIG. 29-2 I2C bus device hooking diagram

29.2. Communication I2C interface signal

Start signal (START):

Under the master mode, the SCL is high potential. The SDA sent from high potential to low potential to enable the data transmission.

DATA and ADDRESS signals:

I2C serial interface protocol is only needed when the SCL is low potential; The SDA can be changed only according to the data.

Acknowledge signal:

Data reception (Slave) starts right after the initial 8 bits.

Transmitting data to the device (Host) is to send a low potential, which means the data are received.

STOP signal:

Under the master mode, the SCL is high potential. The SDA sent from low potential to high potential to end the data transmission.

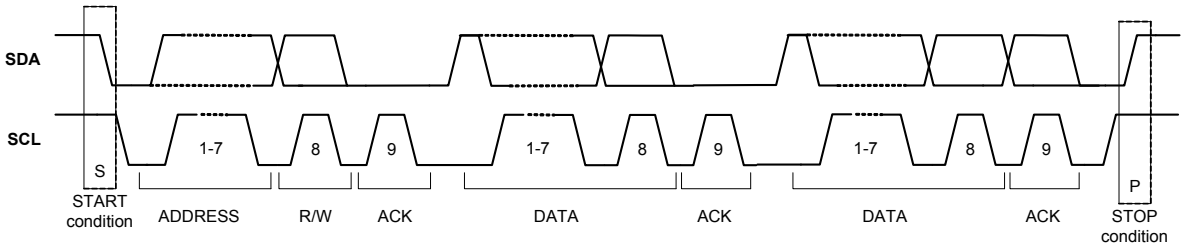

FIG. 29-3 I2C bus clock diagram

Data transmission rate calculation:
The I2C internal register CRG [7:0] can control the data transmission rate of the master mode. The CRG [7:0] value of the internal counter generates a master mode via the signals of the SCL pin, such that the data transmission rate can be based on the frequency of the I2C clock source 2C_CK.

The data transmission of the SCL pin of the I2C bus is clock signal, which is determined by the CRG of the clock source frequency I2CLK of the I2C circuit according to the clock rate of the SCI pin and the following equation:

Data Baud Rate = (I2CLK) / [4X (CRG + 1)] (Equation 29-1)

Timing function (Time-Out):
Timing function is to prevent the I2C controller from locking the I2C communication bus when the I2C works in order to provide enough time to deal with the MCU I2C controller. Therefore, the response of the I2C controller to each bit will occur only after the SCL is reduced to low potential; at this time, the master end cannot receive the next clock signal; in other word, a clock stretching takes place. However, when the MCU is too busy or cannot reply to he I2C controller for other reasons, the SCL I2C communication bus may be locked under the low potential.

In order to prevent from the above situation, the time-out controller will determine whether the SCL status is under low potential time-out according to the frequency divider DI2C [2:0] and time condition controller I2CTLT [3:0].

The condition treatment has the following states:
When the machine detects the SCL is drawn to the low potential and conforms to the condition, the SCL I2C controller will be forced to let go and send an interrupt event to the CPU.

When the SCL fails to conform to the time-out condition and under high potential, the internal counter of the time-out controller will be reset and the next SCL is drawn to low potential to restart the counting.

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I2C communication pin

The I2C bus only has two wires, but the chip allocates 8 sets of communication IO pins for the I2C module (Each set of IO pins includes SCL/SDA), which is for the reuse functions of the IO port. In this way, users can conveniently select different communication pins. The corresponding communication pins can be selected and enabled via the controllers I2CPTS[2:0], I2CPTEN. When using the functions of the I2C, the communication IO pins should be enabled, and the corresponding IO pin should be set under the input mode or output mode. The following table is the communication pin distribution table.

I2CPTS[2:0]	I2CPTEN	SCL	SDA	I2CPTS[2:0]	I2CPTEN	SCL	SDA
000	1	PT1.0	PT1.1	100	1	PT2.0	PT2.1
001	1	PT1.2	PT1.3	101	1	PT2.2	PT2.3
010	1	PT1.4	PT1.5	110	1	PT2.4	PT2.5
011	1	PT1.6	PT1.7	111	1	PT2.6	PT2.7

Table 29-1 I2C communication IO pin distribution

29.2.1. Communication I2C interface flow

I2C serial interface terms

(SPIA): It means giving instructions to the Action control register, where S is the Start instruction, and P is the Stop instruction, I is the interrupt flag and A is the Acknowledge instruction.

SPIA: It means reading the value of the Action control register, which can be used to determine the interrupt flag or other instructions are finished or not.

STA: It means reading the value of the Status register, which is used to show the current operating status of the I2C circuit.

The following flow chart will respectively express the statuses of the I2C interface by (circular frame with gray background), (circular frame with white background) and (white rectangular frame):

Error! An object cannot be established by editing the function variable code.

Circular frame with gray background: it means the I2C status that the interrupt flag is established.

Circular frame with white background: it means the I2C status that the interrupt flag is not established and needs to be read actively by the MCU.

White rectangular frame: it means the instructions to the I2C should be given by the MCU.

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29.2.2. I2C Master TX flow

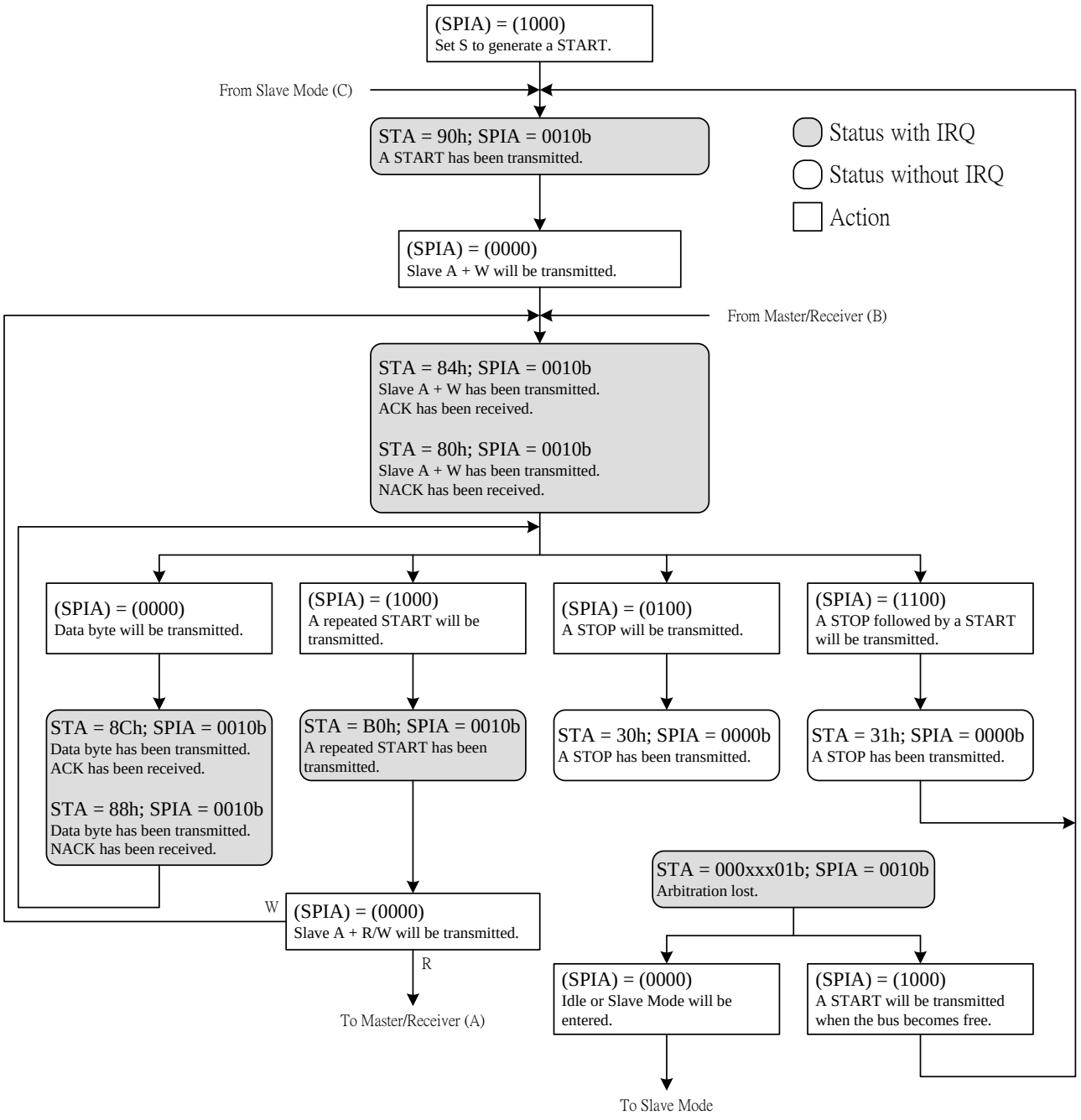
(SPIA) = (1000)
Set S to generate a START.
From Slave Mode (C)
STA = 90h; SPIA = 0010b
A START has been transmitted.
Status with IRQ
Status without IRQ
Action
(SPIA) = (0000)
Slave A + W will be transmitted.
From Master/Receiver (B)
STA = 84h; SPIA = 0010b
Slave A + W has been transmitted.
ACK has been received.
STA = 80h; SPIA = 0010b
Slave A + W has been transmitted.
NACK has been received.
(SPIA) = (0000)
Data byte will be transmitted.
(SPIA) = (1000)
A repeated START will be transmitted.
(SPIA) = (0100)
A STOP will be transmitted.
(SPIA) = (1100)
A STOP followed by a START will be transmitted.
STA = 8Ch; SPIA = 0010b
Data byte has been transmitted.
ACK has been received.
STA = 88h; SPIA = 0010b
Data byte has been transmitted.
NACK has been received.
STA = B0h; SPIA = 0010b
A repeated START has been transmitted.
STA = 30h; SPIA = 0000b
A STOP has been transmitted.
STA = 31h; SPIA = 0000b
A STOP has been transmitted.
STA = 000xxx01b; SPIA = 0010b
Arbitration lost.
W
(SPIA) = (0000)
Slave A + R/W will be transmitted.
R
To Master/Receiver (A)
(SPIA) = (0000)
Idle or Slave Mode will be entered.
(SPIA) = (1000)
A START will be transmitted when the bus becomes free.
To Slave Mode

FIG. 29-4 Master Transmitter Mode

29.2.3. I2C Master RX flow

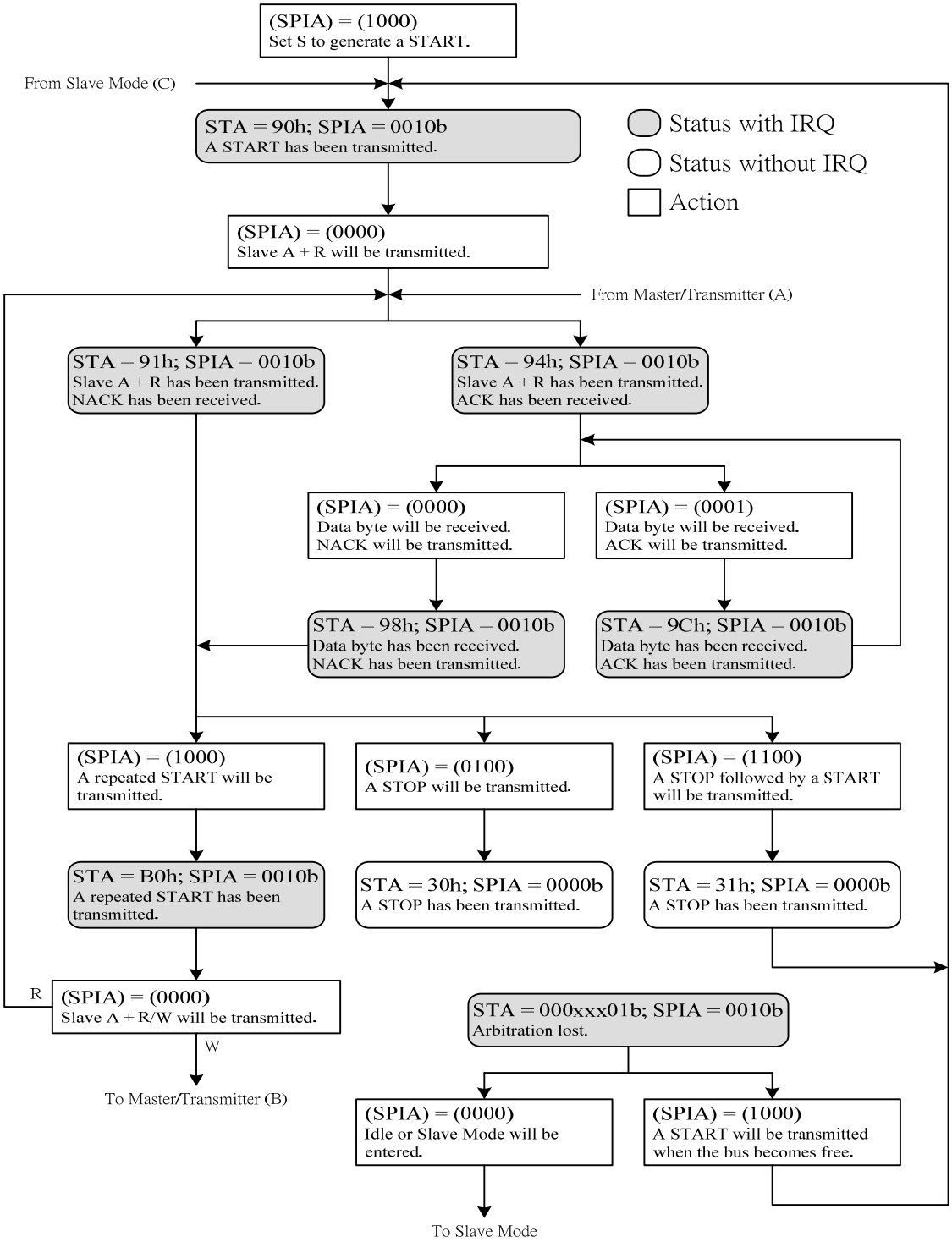
(SPIA) = (1000)
Set S to generate a START.
From Slave Mode (C)
STA = 90h; SPIA = 0010b
A START has been transmitted.
Status with IRQ
Status without IRQ
Action
(SPIA) = (0000)
Slave A + R will be transmitted.
From Master/Transmitter (A)
STA = 91h; SPIA = 0010b
Slave A + R has been transmitted.
NACK has been received.
STA = 94h; SPIA = 0010b
Slave A + R has been transmitted.
ACK has been received.
(SPIA) = (0000)
Data byte will be received.
NACK will be transmitted.
(SPIA) = (0001)
Data byte will be received.
ACK will be transmitted.
STA = 98h; SPIA = 0010b
Data byte has been received.
NACK has been transmitted.
STA = 9Ch; SPIA = 0010b
Data byte has been received.
ACK has been transmitted.
(SPIA) = (1000)
A repeated START will be transmitted.
(SPIA) = (0100)
A STOP will be transmitted.
(SPIA) = (1100)
A STOP followed by a START will be transmitted.
STA = B0h; SPIA = 0010b
A repeated START has been transmitted.
STA = 30h; SPIA = 0000b
A STOP has been transmitted.
STA = 31h; SPIA = 0000b
A STOP has been transmitted.
R
(SPIA) = (0000)
Slave A + R/W will be transmitted.
W
To Master/Transmitter (B)
STA = 000xxx01b; SPIA = 0010b
Arbitration lost.
(SPIA) = (0000)
Idle or Slave Mode will be entered.
(SPIA) = (1000)
A START will be transmitted when the bus becomes free.
To Slave Mode

FIG. 29-5 Master Receiver Mode

29.2.4. I2C Slaver TX flow

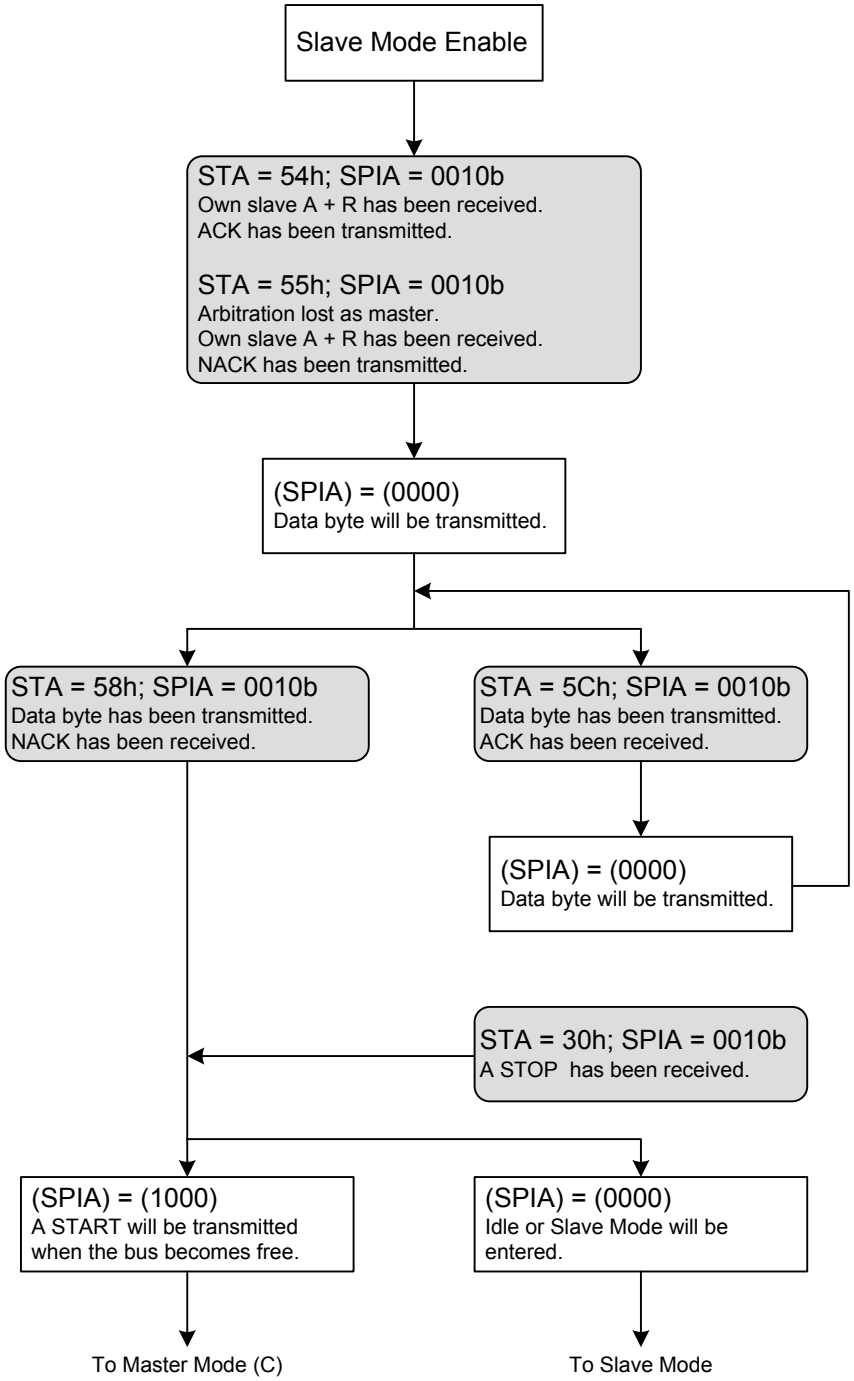
Slave Mode Enable
STA = 54h; SPIA = 0010b
Own slave A + R has been received.
ACK has been transmitted.
STA = 55h; SPIA = 0010b
Arbitration lost as master.
Own slave A + R has been received.
NACK has been transmitted.
(SPIA) = (0000)
Data byte will be transmitted.
STA = 58h; SPIA = 0010b
Data byte has been transmitted.
NACK has been received.
STA = 5Ch; SPIA = 0010b
Data byte has been transmitted.
ACK has been received.
(SPIA) = (0000)
Data byte will be transmitted.
STA = 30h; SPIA = 0010b
A STOP has been received.
(SPIA) = (1000)
A START will be transmitted
when the bus becomes free.
(SPIA) = (0000)
Idle or Slave Mode will be
entered.
To Master Mode (C)
To Slave Mode

FIG. 29-6 Slave Transmitter Mode

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29.2.5. I2C Slaver RX flow

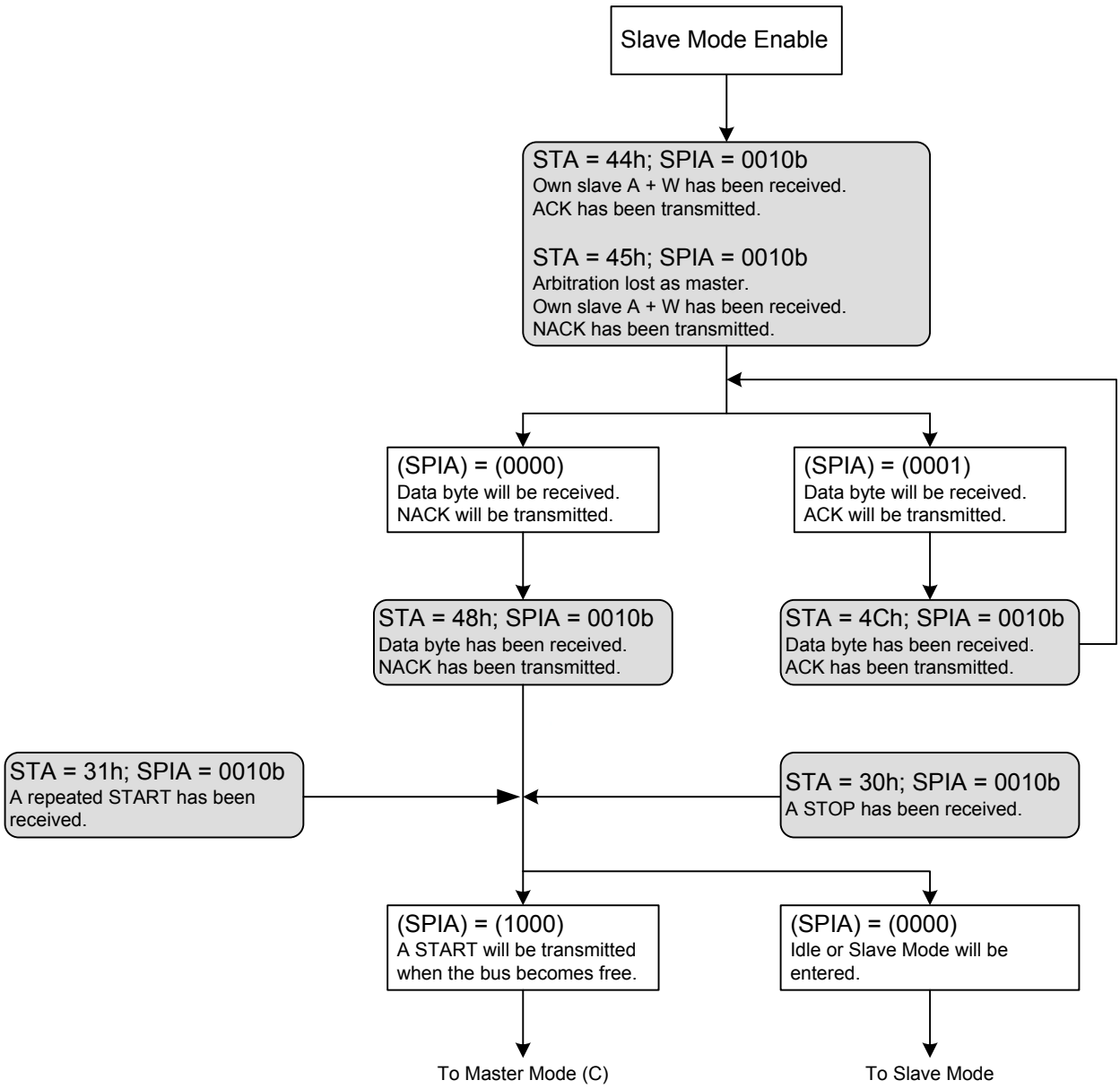
Slave Mode Enable
STA = 44h; SPIA = 0010b
Own slave A + W has been received.
ACK has been transmitted.
STA = 45h; SPIA = 0010b
Arbitration lost as master.
Own slave A + W has been received.
NACK has been transmitted.
(SPIA) = (0000)
Data byte will be received.
NACK will be transmitted.
(SPIA) = (0001)
Data byte will be received.
ACK will be transmitted.
STA = 48h; SPIA = 0010b
Data byte has been received.
NACK has been transmitted.
STA = 4Ch; SPIA = 0010b
Data byte has been received.
ACK has been transmitted.
STA = 31h; SPIA = 0010b
A repeated START has been received.
STA = 30h; SPIA = 0010b
A STOP has been received.
(SPIA) = (1000)
A START will be transmitted when the bus becomes free.
(SPIA) = (0000)
Idle or Slave Mode will be entered.
To Master Mode (C)
To Slave Mode

FIG. 29-7 Slave Receiver Mode

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29.2.6. I2C General Call flow

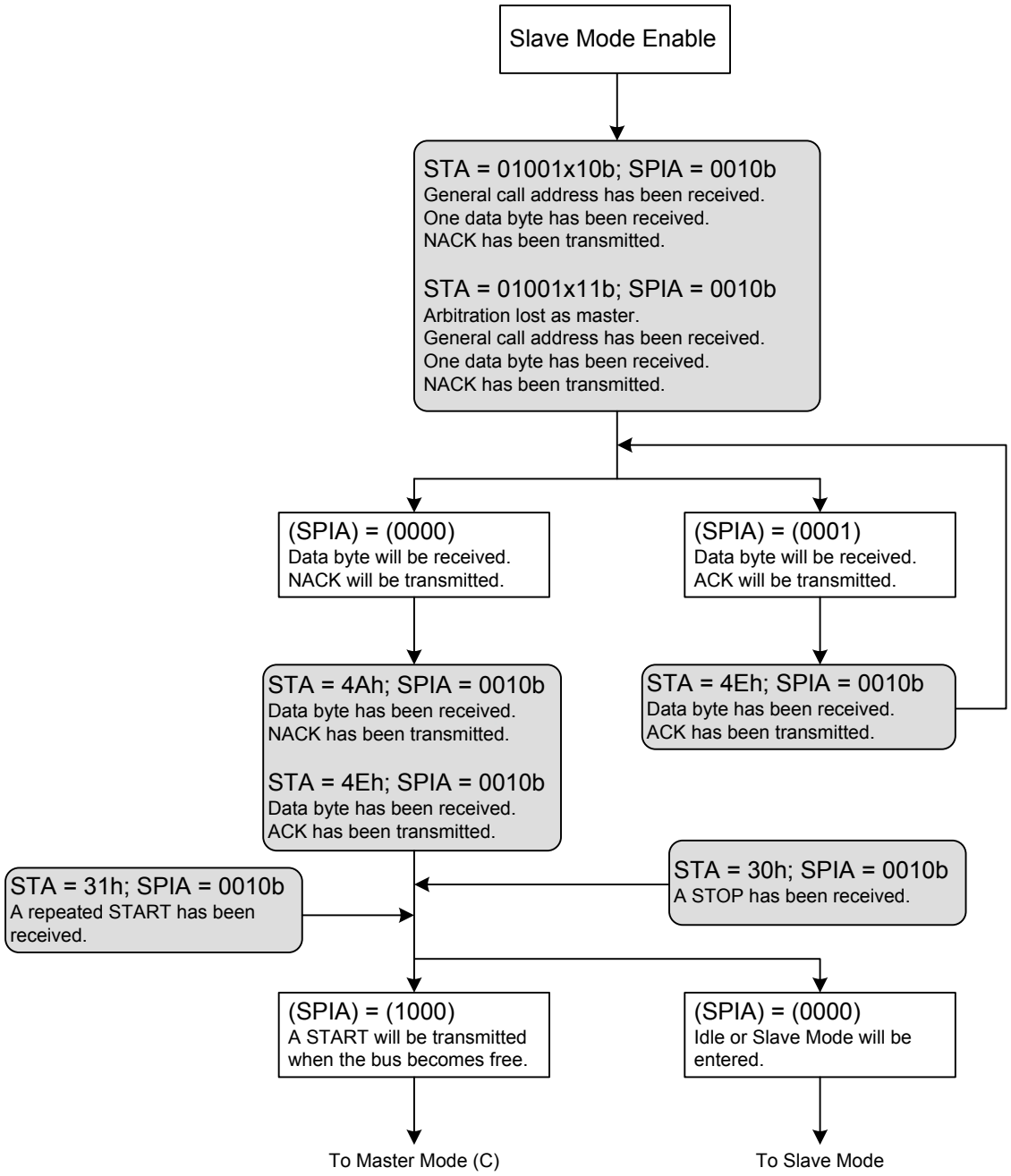
Slave Mode Enable
STA = 01001x10b; SPIA = 0010b
General call address has been received.
One data byte has been received.
NACK has been transmitted.
STA = 01001x11b; SPIA = 0010b
Arbitration lost as master.
General call address has been received.
One data byte has been received.
NACK has been transmitted.
(SPIA) = (0000)
Data byte will be received.
NACK will be transmitted.
(SPIA) = (0001)
Data byte will be received.
ACK will be transmitted.
STA = 4Ah; SPIA = 0010b
Data byte has been received.
NACK has been transmitted.
STA = 4Eh; SPIA = 0010b
Data byte has been received.
ACK has been transmitted.
STA = 4Eh; SPIA = 0010b
Data byte has been received.
ACK has been transmitted.
STA = 31h; SPIA = 0010b
A repeated START has been received.
STA = 30h; SPIA = 0010b
A STOP has been received.
(SPIA) = (1000)
A START will be transmitted when the bus becomes free.
(SPIA) = (0000)
Idle or Slave Mode will be entered.
To Master Mode (C)
To Slave Mode

FIG. 29-8 General Call Mode

29.3. Register address

I2C Register Address	31 24	23 16	15 8	7 0
I2C Base Address + 0x00 (0x41000)	-	-	MASK0	I2C_CON0
I2C Base Address + 0x04 (0x41004)	MASK1	I2C_CON1	MASK2	I2C_CON2
I2C Base Address + 0x08 (0x41008)	MASK3	I2C_CON3	MASK4	I2C_CON4
I2C Base Address + 0x0C (0x4100C)	MASK5	MASK6	I2C_CON5	I2C_CON6
I2C Base Address + 0x10 (0x41010)	-	-	-	I2C_CON7
I2C Base Address + 0x14 (0x41014)	-	-	-	I2C_CON8

-Reserved

29.4. Register function

29.4.1. I2C register 0

I2C Base Address + 0x00 (0x41000)					
Symbol	I2CCR0 (I2C Control Register 0)				
Bit	[31:16]				
Name	RSV.				
RW	R-0				
Bit	[15:8]	[7:3]	[2]	[1]	[0]
Name	MASK	RSV.	GCRst	TOEn	I2CEn
RW	R0W-0	R-0	RW-0		

Bit	Name	Description	
Bit[02]	GCRst	General calling reset enable control	
		0	Disable
		1	Enable
Bit[01]	TOEn	Time-out reset function enable control	
		0	Disable
		1	Enable
Bit[00]	I2CEn	I2C function enable control	
		0	Disable
		1	Enable

29.4.2. I2C register 1

Action Register (ACT)

I2C Base Address + 0x04 (0x41004)									
Symbol	I2CCR1 (I2C Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	MAct	SAct	Rx P/Sr	R/W	DF	A/NA	GC	ARB
RW	R0W-0	R-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	SEn	10bEn	3BEn	EIRQFlag	START	STOP	IRQFlag	A/NA
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23]	MAct	Master mode enable flag	
		0	Disable
		1	Enable
Bit[22]	SAct	Slave mode enable flag	
		0	Disable
		1	Enable
Bit[21]	Rx P/Sr	Reception stop or restart flag	
		0	Normal
		1	The reception stop or restart flag has been sent or received
Bit[20]	R/W	Read/write status flag	
		0	The writing instruction has been sent or received.
		1	The reading instruction has been sent or received.
Bit[19]	DF	Data flag	
		0	Normal
		1	The I2C data have been sent or received.
Bit[18]	A/NA	Response signal (ACK) status flag	
		0	The response signal (ACK) has yet to be sent or received.
		1	The response signal (ACK) has been sent or received.
Bit[17]	GC	General calling status flag	
		0	Normal
		1	The general calling operation is performed now.
Bit[16]	ARB	Arbitration loss flag	
		0	Normal
		1	Arbitration loss
Bit[07]	SEn	Slave mode enable control	
		0	Disable
		1	Enable
Bit[06]	10bEn	Slave 10-bit address code mode enable control	
		0	Disable
		1	Enable the 10-bit address code mode
Bit[05]	3BEn	Slave sending 3 pieces of data function enable control	
		0	Disable
		1	Enable the slave continuously sending 3 pieces of data function.

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Bit[04]	EIRQ Flag	Error flag, related to the error interrupt flag I2CEIF; the I2CEIF can be cleared after the bit is cleared.	
		0	Normal
		1	The time-out or receiving accidental start (stop) signal or arbitration failure takes place.
Bit[03]	STAR T(S)	(S) Start signal control bit	
		0	Normal
		1	Generate the start signal from the I2C bus.
Bit[02]	STOP (P)	(P) Stop signal control bit	
		0	Normal
		1	Generate the stop signal from the I2C bus.
Bit[01]	IRQFl ag(I)	(I) Interrupt control bit	
		0	Normal;
		1	Reply to the interrupt; the device will reply to the interrupt after receiving 9 clocks, and then draw the SCL to low potential until the bit is cleared and release the SCL signal wire; writing in 0 will clear the device status control bit and make the I2C proceed to the next status.
Bit[00]	A/NA(A)	(A) Response signal replying control bit	
		0	Fail to reply to the ACK or reply to NACK.
		1	The response signal (ACK) has been replied.

25.3.4 I2C register 2

I2C Base Address + 0x08 (0x41008)				
Symbol	I2CCR2 (I2C Control Register 2)			
Bit	[31:24]	[23:16]		
Name	MASK	CRG		
RW	R0W-0	RW-0		
Bit	[15:08]	[7]	[6:4]	[3:0]
Name	MASK	TOFlag	TOPS	TOLimit
RW	R0W-0	R-0	RW-0	

Bit	Name	Description	
Bit[23~16]	CRG	I2C bus data serial transmission rate control register	
		0	Reserved
		1	Set 1

The data serial transmission rate of the I2C bus is determined by the values of the clock source of the I2C and the serial transmission rate control register CRG; the data serial transmission rate of the I2C bus can be calculated according to the following equation:

Data Baud Rate = (I2CLK) / [4x (CRG + 1)]

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Bit	Name	Description	
Bit[7]	TOFlag	Time-out flag	
		0	Normal
		1	The I2C bus clock wire high/low potential control is overtimed.
Bit[6~4]	TOPS	Time-out clock frequency divider configuration	
		111	CLKPS = I2CLK / 128
		110	CLKPS = I2CLK / 64
		101	CLKPS = I2CLK / 32
		100	CLKPS = I2CLK / 16
		011	CLKPS = I2CLK / 8
		010	CLKPS = I2CLK / 4
		001	CLKPS = I2CLK / 2
		000	CLKPS = I2CLK / 1
Bit[3~0]	TOLimit	Time-out upper limit configuration	
		1111	16x CLKPS Cycle
		1110	15x CLKPS Cycle
		1101	14x CLKPS Cycle
		1100	13x CLKPS Cycle
		1011	12x CLKPS Cycle
		1010	11x CLKPS Cycle
		1001	10x CLKPS Cycle
		1000	9x CLKPS Cycle
		0111	8x CLKPS Cycle
		0110	7x CLKPS Cycle
		0101	6x CLKPS Cycle
		0100	5x CLKPS Cycle
		0011	4x CLKPS Cycle
		0010	3x CLKPS Cycle
		0001	2x CLKPS Cycle
		0000	1x CLKPS Cycle

29.4.3. I2C register 3

Slave ID0 (SID0)

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I2C Base Address + 0x0C (0x4100C)				
Symbol	I2CCR3 (I2C Control Register 3)			
Bit	[31:24]		[23:16]	
Name	SID1 MASK		SID0 MASK	
RW	R0W-0		R0W-0	
Bit	[15:9]	[8]	[7:1]	[0]
Name	SID1	VD1	SID0	VD0
RW	RW-0		RW-0	

Bit	Name	Description	
Bit[31~24]	SID1 MASK	SID1 MASK	
		0	Disable
		1	Enable
Bit[23~16]	SID0 MASK	SID0 MASK	
		0	Disable
		1	Enable
Bit[15~9]	SID1	SID1 slave address code configuration	
		0	Set 0
		1	Set 1
Bit[08]	Valid1	Slave address code valid control bit, the bit should be 1 when writing in the address code.	
		0	The slave address code is invalid.
		1	The slave address code is valid.
Bit[7~1]	SID0	SID0 slave address code configuration	
		0	Set 0
		1	Set 1
Bit[00]	Valid0	Slave address code valid control bit, the bit should be 1 when writing in the address code.	
		0	The slave address code is invalid.
		1	The slave address code is valid.

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29.4.4. I2C register 4

I2C Base Address + 0x10 (0x41010)			
Symbol	I2CCR4 (I2C Control Register 4)		
Bit	[31:16]		
Name	RSV.		
RW	R-0		
Bit	[15:8]	[7:1]	[0]
Name	RSV	Rx A7-1/D7-1	RW/D0
RW	R-0	R-X	

Bit	Name	Description	
Bit[7~1]	Rx A7-1/D7-1	Register RX[7:0] for receiving address or data	
		0	Set 0
		1	Set 1
Bit[0]	RW/D0	The received data is the 0th value of the read/write instruction or data.	
		0	Set 0
		1	Set 1

29.4.5. I2C register 5

Transmitter Data Buffer 0 (TXAD)

I2C Base Address + 0x14 (0x41014)			
Symbol	I2C 5 (I2C Control Register 5)		
Bit	[31:24]	[23:17]	[16]
Name	RSV.	TX2 A7-1/D7-1	Flag/D0
RW	R-0	RW-X	
Bit	[15:08]	[7:1]	[0]
Name	TX1 A7-0/D7-0	TX0 A7-1/D7-1	RW/D0
RW	RW-X		

Bit	Name	Description	
Bit[23~17]	TX2 A7-1/D7-1	Transmission register 2 for transmitting the address or the value of the data[7:1]	
		0	Set 0
		1	Set 1
Bit[16]	Flag/D0	Transmission register 2 for transmitting the read/write instruction or the value of the data[0]	
		0	Set 0
		1	Set 1
Bit[15~8]	TX1 A7-0/D7-0		

Transmission register 1 for transmitting the address

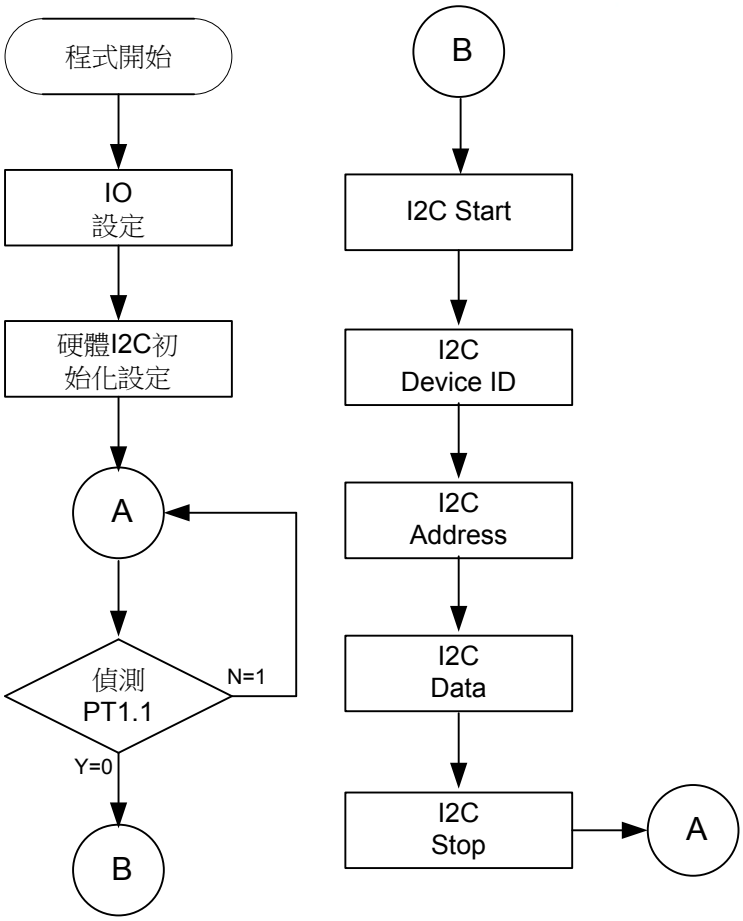
		or the value of the data[7:0]	
		0	Set 0
		1	Set 1
Bit[7~1]	TX0 A7-1/D7-1	Transmission register 0 for transmitting the address or the value of the data[7:1]	
		0	Set 0
		1	Set 1
Bit[00]	RW/D0	Transmission register 0 for transmitting the read/write instruction or the value of the data[0]	
		0	Set 0
		1	Set 1

Note:

During the communication process, when no data are transmitted, the data transmission register should be set as 0xFF/

Because the SDA bus tends to be locked at 0 when the lowest bit is drawn to low for a long time.

29.5. Model program flow



The program starts
IO settings
Hardware I2C initialization settings
Detect

29.6. Model program function

Model name: test the hardware I2C
Model description:
Test the write-in function of the hardware I2Cto the AT24C02 via the settings of the I2C pins and the I2C register.

29.7. Model program description

(Main program)

```
00
01  #include "HY16F19X.h"
02
03
04  volatile unsigned int i,a;
05
06
07  int main(void)
08  {
09     I2C_INI();
11
12     while(1)
13     {
14          i=DrvGPIO_GetBit(E_PT1,1);          //read PT1.1 pin high or low
15          while(i==0)
16          {
17               I2C_Start();                   //Hardware I2C Start
18
19               DrvI2C_WriteData(0xA0);        //AT24C02 Device ID
20               I2C_NACK();
21
22               DrvI2C_WriteData(0x00);        //AT24C02 Address=0x00
23               I2C_NACK();
24
25               DrvI2C_WriteData(0x55);        //Data1=0x55 @ Address=0x00
26               I2C_NACK();
27
28               DrvI2C_WriteData(0xAA);        //Data2=0xAA @ Address=0x01
29               I2C_NACK();
30
31               I2C_Stop();                    //Hardware I2C Stop
32
33               I=1;
34          }
35          Delay(0x50);
36      }
37     return 0;
38  }
```

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(Subprogram)

```
00
01  void I2C_INI(void)                                  //Hardware I2C Initial
02  {
03     DrvGPIO_Open(E_PT1,0x06,E_IO_INPUT);             //PT1.1 input
04     DrvGPIO_Open(E_PT1,0xf6,E_IO_PullHigh );
05
06
07
08     pio_44=0x0b0bFF00;
09     i2c_00=0xFF00FF00;                               //0x41000//I2C OFF
11     i2c_14=0x0000FFFF;                               //0x44014
12  }
13
14
15  void I2C_Start(void)                                //Hardware I2C Start
16  {
17     DrvI2C_Ctrl(1,0,0,0);                            //SPIA(1000)
18     I2C_NOP();
19  }
20
21  void I2C_Stop(void)                                 //Hardware I2C Stop
22  {
23     DrvI2C_Ctrl(0,1,0,0);                            //SPIA(0100)
24     I2C_NOP();
25  }
26
27  void I2C_Write(unsigned int I2C_Data)               //Hardware I2C Write
28  {
29     DrvI2C_WriteData(I2C_Data);
30     i2c_04=0xFF01;                                   //0x41004
31     I2C_NOP();
32  }
33
34  void I2C_NACK(void)                                 //Hardware I2C NACK
35  {
36     DrvI2C_ClearIRQ();
37     DrvI2C_ClearEIRQ();
38     while(!(i2c_04 & 0x00000002));
39  }
40
41  void I2C_NOP(void)                                  //Software I2C NOP
42  {
43     volatile unsigned int n;
44     for(n=0;n<=0x10;n++);asm("NOP");//0x10
45  }
46
```

30. HARDWARE REAL TIME CLOCK (HW RTC)

30.1. Overall description

The real time clock controller provides the real time clock and calendar.
The clock source of the RTC is from the external 32.768 KHz crystal connected to the I/O port or the internal 35kHz LPO oscillator.
The RTC controller shows the time information about hour/minute/second by binary coded decimal (BDC) and the calendar information about year/month/day.
The controller has a programmable alert interrupt program and a periodically programmable wake-up interrupt program, such that the system can be automatically wakened to deal with the low power mode. The controller further has a 6-bit digital timing crystal oscillator offset compensation mechanism.

Function: The time information (hour/minute/second) and the date information (year/month/day) are stored in the register.
Alert register (year/month/day/hour/minute/second)
All time and date information are shown by the BCD format.
Leap automatic compensation (years: 2012~2099)
Week counter
6-bit digital timing crystal oscillator offset compensation
Support periodically wake up the CPU from the idle mode.
Support 8 periodical wake-up period options: 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, and 1
Support two time modes, 12/24 systems.

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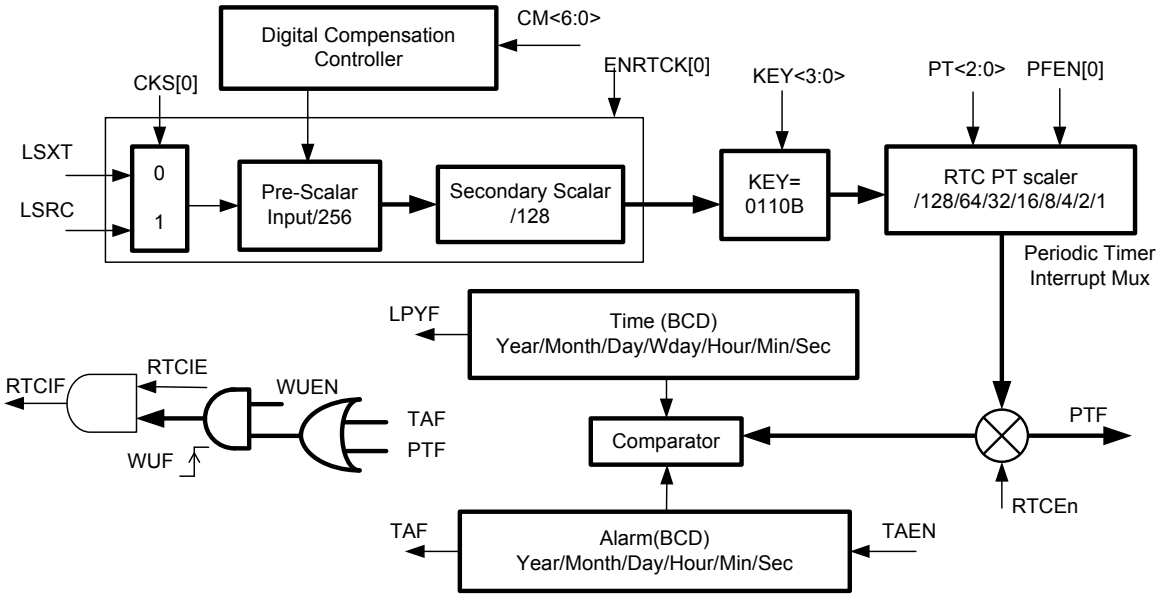

FIG. 30-1 RTC structure diagram

Access the RTC register:

The frequency of the RTC clock is different from that of the system clock; thus the register will be updated after two RTC clock pulses if the user has written new data in the register. The RTC data should be updated frequently.

A protection button for writing data in the register is provided.

When writing data in the RTC register, the RTKEY button should be set as <0110>, and other values of the RTKEY button will not allow any data to be written in the RTC register. Please note that the RTC will not check the data format written in the register; thus, the user should be extremely careful with the write-in operation.

Enable the RTC:

It is necessary to write <0110> in the RTKEY before writing data into the RTC register.

If the user wants to enable the RTC, the user should check whether the LPOSC or LS_CLK can be used first. Then, set the RTCEN as 1.

Frequency compensation:

The RTC allows the digital compensation for the clock input. The central frequency of the RTC is 32768Hz.

Any imperfect operations may result in the frequency offset. The digital compensation can be used to reduce the frequency offset.

The compensation method is to execute +/-2ppm at each step; the permissible maximal frequency change is +126ppm, and the permissible minimal frequency change is -126ppm. The maximal input frequency is 32772Hz, and the minimal input frequency is 32763Hz.

The maximal reference frequency that the user can input is 16MHz to measure the RTC clock during the manufacturing period.

The measurement value is calculated to obtain the compensation value. Then, the compensation value will be stored in the flash memory.

Once the system starts up, the compensation value will be loaded into the RTCO<6:0>.

Time information:

The time information is stored in the RTHR/RTMI/RTSE registers, which use BCD format.

The user can set the time as the 24 hour system or 12 hour (AM/PM) system.

The time default value is 00:00:00 (hour/minute/second), and it is 24 hour system.

Calendar information:

The calendar information is stored in the RTYE/RTMO/RTDA/RTWDA registers, which use BCD format. The algorithm for leap year is performed by the hardware.

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The effective year period is between 2012~2099. If the RTLPYF is 1, it is the leap year. The year is expressed by two digits, which stands for 20xX year. The default date after the system is reset is 12/1/1 Sunday (January 2, 2012).
The maximal year is 99; and the year will become 00/1/1 after 99/12/31; but the leap year compensation will fail if the above condition takes place.

Week counter:
The RTC controller provides the information about one week. The WDA value is defined from 0 to 6, which stands for Sunday to Saturday respectively.

Alert interrupt:
If the registers, RTYE/RTMO/RTDA/RTHR/RTMI/RTSE, conform to the registers, RCYE/RCMO/RCDA/RCHR/RCMI/ RCSE and the RTAEN is 1, the RTTAF interrupt flag will be set as 1 to MCU.

Periodic timer interrupt:
The periodic timer has 8 periodic options for interrupt: 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
Set the RTPFEN as 1 to enable the periodic timer interrupt. These periodic options are controlled by the RTPT<2:0>.

System wake-up interrupt:
When the MCU enters the idle mode, it can be wakened by the system wake-up interrupt program.
There are two sources able to wake up the MCU: the periodic timer interrupt and alert interrupt. Set the RTWFEN as 1 to enable the interrupt program.

30.2. Register address

RTC Register Address	31 24	23 16	15 8	7 0
RTC Base Address + 0x00 (0x41A00)	RTKEY	RTCC1	RTCC0M	RTCC0
RTC Base Address + 0x04 (0x41A04)	RTCOM	RTCO	RTCPTM	RTPT
RTC Base Address + 0x08 (0x41A08)	-	-	RTHRM	RTHR
RTC Base Address + 0x0C (0x41A0C)	RTMIM	RTMI	RTSEM	RTSE
RTC Base Address + 0x00 (0x41A10)	RTYEM	RTYE	RTMOM	RTMO
RTC Base Address + 0x04 (0x41A14)	RTDAM	RTDA	RTWDM	RTWDA
RTC Base Address + 0x08 (0x41A18)	-	RCHR	RCMI	RCSE
RTC Base Address + 0x0C (0x41A1C)	-	RCYE	RCMO	RCDA

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-Reserved

30.3. Register function

30.3.1. Hardware RTC register RTCCR0

RTC Base Address + 0x00 (0x41A00)									
Symbol	RTCCR0 (RTC Control Register 0)								
Bit	[31:28]	[27:24]	[23:20]			[19]	[18]	[17]	[16]
Name	-	MASK	KEY			LPYF	PTF	WUF	TAF
RW	-	R0W-0	RW-0			R-0	RW0-0	R-0	RW0-0
Bit	[15:14]	[13:8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	MASK	-	PTEn	WUEn	TAEn	HRF	CKS	RTCEn
RW	-	R0W-0	-	RW-0					

Bit	Name	Description	
Bit[23-20]	KEY	The secret key of the RTC register; it can be locked to protect the register to prevent data from being written in the register.	
		0110	The write-in secret key; it can lift the protection of the register, and data can be written in the register only after it is unlocked.
		Others	Lock the register to protect it; no data can be written in the register.
Bit[19]	LPYF	Leap year flag	
		0	The current year is not a leap year.
		1	The current year is a leap year.
Bit[18]	PTF	Timer wake-up interrupt flag	
		0	Normal
		1	Timer wake-up is triggered.
Bit[17]	WUF	Wake-up interrupt flag	
		0	Normal
		1	The wake-up interrupt is triggered.
Bit[16]	TAF	Alarm clock status flag	
		0	Normal
		1	The alarm interrupt is triggered.
Bit[05]	PFEN	RTC timer timing function enable control	
		0	Disable
		1	Enable

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Bit[04]	WUFEN	RTC wake-up function enable control	
		0	Disable
		1	Enable
Bit[03]	TAEN	RTC alarm clock function enable control	
		0	Disable
		1	Enable
Bit[02]	HRF	RTC hour format configuration (24/12)	
		0	12 hour system (PM/AM)
		1	24 hour system
Bit[01]	CKS	RTC clock source input selection	
		0	External low-speed crystal oscillator source
		1	Internal low-speed crystal oscillator source
Bit[00]	RTCEN	RTC function enable control	
		0	Disable the function of the RTC.
		1	Enable the function of the RTC

30.3.2. Hardware RTC register RTCCR1

RTC Base Address + 0x04 (0x41A04)						
Symbol	RTCCR1 (RTC Control Register 1)					
Bit	[31]	[30:24]	[23]	[22:16]		
Name	-	MASK	-	CM		
RW	-	R0W-0	-	RW-0		
Bit	[15:08]		[7:5]	[4]	[3]	[2:0]
Name	MASK		-	CKH	-	PT
RW	R0W-0		-	RW-0	-	RW-0

Bit	Name	Description	
Bit[22~16]	CM	RTC clock frequency compensation value configuration	
		0111111	+126 PPM crystal oscillator frequency compensation (maximum)
		0111110	+124 PPM crystal oscillator frequency compensation
		…	Incremental step: +2 PPM crystal oscillator frequency compensation
		0000001	+2 PPM crystal oscillator frequency compensation
		0000000	0 PPM crystal oscillator frequency compensation
		1000000	0 PPM crystal oscillator frequency compensation
		1000001	-2 PPM crystal oscillator frequency compensation
		…	Decremental step: -2 PPM crystal oscillator frequency compensation

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		1111110	-124 PPM crystal oscillator frequency compensation
		1111111	-126 PPM crystal oscillator frequency compensation (minimum)
Bit[4]	CKH	RTC high-speed clock source enable control; it is suggested that the function be enabled under the test mode.	
		0	Disable; the low-speed clock source is used.
		1	Enable; the high-speed clock source is used.
Bit[2~0]	PT	Timer timing wake-up time configuration	
		000	1/128 s
		001	1/64 s
		010	1/32 s
		011	1/16 s
		100	1/8 s
		101	1/4 s
		110	1/2 s
		111	1 s

30.3.3. Hardware RTC register RTCHRC

RTC Base Address + 0x08 (0x41A08)					
Symbol	RTCHRC (RTC Hour Control Register For calendar)				
Bit	[31:15]				
Name	RSV				
RW	R-0				
Bit	[14:08]	[7]	[6]	[5:4]	[3:0]
Name	MASK	-	PM	10HR	1HR
RW	R0W-0	-	RW-0		

Bit	Name	Description	
Bit[6]	HRPM	Real time clock hour format am/pm	
		0	AM or 24 hour system
		1	PM (it should be set as 1 if, the HRF is set as 1.)
Bit[5~4]	10HR	The tens place of the hour (BCD code format)	
		00	0
		01	1
		10	When 2 (HRF=1) / HRF=0, it is invalid.
		11	Invalid

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Bit[3~0]	1HR	The one's place of the hour (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid

30.3.4. Hardware RTC register RTCSMC

RTC Base Address + 0x0C (0x41A0C)				
Symbol	RTCSMC (RTC seconds and min Control Register For calendar)			
Bit	[31:24]	[23]	[22:20]	[19:16]
Name	MASK	-	10MIN	1MIN
RW	R0W-0	-	RW-0	RW-0
Bit	[15:08]	[07]	[06:04]	[03:00]
Name	MASK	-	10SEC	1SEC
RW	R0W-0	-	RW-0	RW-0

Bit	Name	Description	
Bit[22~20]	10MIN	The tens place of the minute (BCD code format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6

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		111	Invalid
Bit[19~16]	1MIN	The one’s place of the minute (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[6~4]	10SEC	The tens place of the second (BCD code format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Invalid
Bit[3~0]	1SEC	The one’s place of the second (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid

30.3.5. Hardware RTC register RTCYMC

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RTC Base Address + 0x10 (0x41A10)				
Symbol	RTCYMC (RTC Year and Month Control Register For Calendar)			
Bit	[31:24]	[23:20]		[19:16]
Name	MASK	10YEAR		1YEAR
RW	R0W-0	RW-1		RW-2
Bit	[15:08]	[07:05]	[04]	[03:00]
Name	MASK	-	10MO	1MO
RW	R0W-0	-	RW-0	RW-1

Bit	Name	Description	
Bit[23~20]	10YEAR	The tens place of the year (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[19~16]	1YEAR	The one’s place of the year (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[4]	10MO	The tens place of the month (BCD code format)	
		0	0
		1	1
Bit[3~0]	1MO	The one’s place of the month(BCD code format)	
		0000	0

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		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid

30.3.6. Hardware RTC register RTCDWC

RTC Base Address + 0x14 (0x41A14)				
Symbol	RTCDWC (RTC Date and week Control Register For calendar)			
Bit	[31:24]	[23:22]	[21:20]	[19:16]
Name	MASK	-	10DAT	1DAT
RW	R0W-0	-	RW-0	RW-1
Bit	[15:08]	[07:03]		[02:00]
Name	MASK	-		WDA
RW	R0W-0	-		RW-0

Bit	Name	Description	
Bit[21~20]	10DAT	The tens place of the date (BCD code format)	
		00	0
		01	1
		10	2
		11	3
Bit[19~16]	1DAT	The one’s place of the month (BCD code format)	
		0000	0
		0001	1

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		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[2~0]	WDA	The value of the Week (BCD code format)	
		000	Sunday
		001	Monday
		010	Tuesday
		011	Wednesday
		100	Thursday
		101	Friday
		110	Saturday
		111	Invalid

30.3.7. Hardware RTC register RTCHRA

RTC Base Address + 0x18(0x41A18)							
Symbol	RTCHRA (RTC Hour and min and seconds Control Register for alarm)						
Bit	[31:24]			[23]	[22]	[21:20]	[19:16]
Name	RSV			-	CPM	10CHR	1CHR
RW	R-0			-	RW-0		
Bit	[15]	[14:12]	[11:8]	[7]	[6:4]	[3:0]	
Name	-	10CMI	1CM1	-	10CSE	1CSE	
RW	-	RW-0		-	RW-0		

Bit	Name	Description	
Bit[22]	CPM	The format of the alarm clock is am/pm.	
		0	AM or 24 hour system
		1	PM (when HRF=1, the bit should be set as 1.)
Bit[21~20]	10CHR	The tens place of the hour under the alarm clock mode (BCD code format)	
		00	0
		01	1
		10	When 2 (HRF=1) / HRF=0, it is invalid.
		11	invalid

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Bit[19~16]	1CHR	The one's place of the hour under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[14~12]	10CMI	The tens place of the minute under the alarm clock mode (BCD code format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Invalid
Bit[11~8]	1CMI	The one's place of the minute under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[6~4]	10CSE	The tens place of the second under the alarm clock mode (BCD code format)	
		000	0
		001	1
		010	2

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		011	3
		100	4
		101	5
		110	6
		111	Invalid
Bit[3~0]	1CSE	The one's place of the second under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid

30.3.8. Hardware RTC register RTCYMDA

RTC Base Address + 0x1C(0x41A1C)						
Symbol	RTCYMDA (RTC Year /month/date Control Register For alarm)					
Bit	[31:24]			[23:20]		[19:16]
Name	RSV			10CYE		1CYE
RW	R-0			RW-1		RW-2
Bit	[15:13]	[12]	[11:8]	[07]	[06:04]	[03:00]
Name	-	10CMO	1CMO	-	10CDAT	1CDAT
RW	-	RW-0	RW-1	-	RW-0	RW-1

Bit	Name	Description	
Bit[23~20]	10CYE	The tens place of the year under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5

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		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[19~16]	1CYE	The one’s place of the year under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid
Bit[12]	10CMO	The tens place of the month under the alarm clock mode (BCD code format)	
		0	0
		1	1

Bit	Name	Description	
Bit[11~8]	1CMO	The one’s place of the month under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Invalid
Bit[5~4]	10CDAT	The tens place of the date under the alarm clock mode (BCD code format)	
		00	0
		01	1

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		10	2
		11	3
Bit[3~0]	1CDAT	The one’s place of the date under the alarm clock mode (BCD code format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Other values	Invalid

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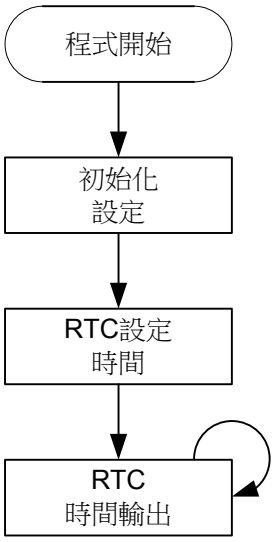
30.4. Model program flow



The program starts.

Initialization settings

RTC time setting

RTC time output

30.5. Model program function

Model name: test the hardware RTC

Model description: test the real time clock function of the hardware RTC

30.6. Model program description

(Main program)

```
01  #include "HY16F19X.h"
02  unsigned int sec,min,hour,week,day,month,year;
03
04  void Delay(unsigned int num);
05  void RTC_Initial(void);
06
07  int main(void)
08  {
09    RTC_Initial();                                  //RTC initialization (including time setting)
11
12    while(1)
13    {
14      asm("NOP");
15                                                    //RTC backward-reading time setting
16      DrvRTC_Read(DRVRTC_CURRENT_TIME,&sCurTime);   //RTC backward-reading time data
17
18      sec=sCurTime.u32cSecond;                      //backward-reading_second
19      min=sCurTime.u32cMinute;                      //backward-reading_minute
20      hour=sCurTime.u32cHour;                       //backward-reading_hour
21      week=sCurTime.u32cDayOfWeek;                  //backward-reading_week
22      day=sCurTime.u32cDay;                         //backward-reading_date
23      month=sCurTime.u32cMonth;                     //backward-reading_month
```

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```
24      year=sCurTime.u32Year;          //backward-reading_year
25      asm("NOP");
26    }
27    return 0;
28  }
29
```

(Subprogram)

```
00
01  void RTC_Initial(void)
02  {
03    //RTC CLK;
04    clk_08=0x8080ff04;
05    //RTC KEY;
06    DrvRTC_WriteEnable();
07    clk_00=0x0404;
08
09
11    //DrvRTC_ClockSource(E_INTERNAL_CLOCK);//35KHz
12    DrvRTC_ClockSource(E_EXTERNAL_CLOCK);//32768Hz
13
14    DrvRTC_PeriodicTimeEnable(0);//set 1/128
15    DrvRTC_Enable();
16    DrvRTC_HourFormat(0);
17
18    asm("NOP");
19    S_DRVRTC_TIME_DATA_T sCurTime;//setting start
20    DrvRTC_Read(DRVRTC_CURRENT_TIME,&sCurTime);
21    sCurTime.u8cClockDisplay=1;
22    sCurTime.u8cAmPm=0;
23    sCurTime.u32cSecond=19;         //setting_second
24    sCurTime.u32cMinute=50;         //setting _munite
25    sCurTime.u32cHour=10;           //setting _hour
26    sCurTime.u32cDayOfWeek=5;       //setting _week
27    sCurTime.u32cDay=9;             //setting _date
28    sCurTime.u32cMonth=8;           //setting_month
29    sCurTime.u32Year=2013;          //setting _year
30    sCurTime.u8IsEnableWakeUp=0;
31    DrvRTC_Write(DRVRTC_CURRENT_TIME,&sCurTime);
32    asm("NOP");
33  }
34
```

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31. POWER-SAVING MODE INTRODUCTION

31.1. Overall description

The paragraph will describe different power modes and their corresponding function modules.

Under the active mode, all peripheral circuits can be enabled, and the clock of the MCU is HS_CK or LS_CK clock; under the mode, the system can freely switch to other modes and have shortest response time.

Under the low-power mode, all analog circuits can be enabled and the clock of the MCU is LS_CK clock; under the mode, the MCU works under the lowest frequency and the system can switch to other modes by executing instructions.

There are four power-saving modes able to make the MCU stop executing instructions. These modes can be disabled by the interrupt. Once the interrupt is triggered, the internal 2MHz clock source will be enabled; then, the MCU will word under the clock source and the system will leave these power-saving modes..

Before entering the power-saving modes, the chip should enable anyone of the interrupt vectors, or the power-saving effect cannot be achieved. In particular, under different power-saving modes, only some function modules can be enabled, and only some functions can waken the chip from the power-saving modes. For example, under the sleep mode, the timer interrupt is invalid, and the chip can be wakened only by the communication interrupt, IO port external interrupt and reset.

31.2. Interrupt point configuration

When the CPU is under different operating modes, the interrupt-triggered items supported by the CPU are also different; the following table shows the interrupt and wake-up levels supported by each function. Similarly, different modes have different current consumption; the current consumption from high to low is: active mode > wait mode > idle mode > sleep mode. For instance, the interrupt function of the I2C TX pin only supports the idle mode, wait mode and active mode. That is to say, after the chip enters the sleep mode, the chip cannot be wakened by the signals of the I2C TX pin to enter the interrupt. For example, after the chip enters the sleep mode, only following actions and interrupts can make the chip leave the sleep mode: Power On Reset, Reset PIN, I2C RX IRQ, UART1/2 RX IRQ, SPI RX IRQ, CMP IRQ, PT1 IRQ and PT2 IRQ, etc.

Interrupt/Reset Mode	Sleep Mode		Idle Mode		Wait Mode		Active Mode		Note
	Enter	leave	Enter	leave	Enter	leave	Enter	leave	
Power On Reset		V		V		V	V	V	Chip Reset
Reset PIN		V		V		V	V	V	Chip Reset

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WDT Reset				V		V	V	V	WDT Reset Type
I2C TX IRQ			V	V	V	V	V	V	I2CIE
I2C RX IRQ	V	V	V	V	V	V	V	V	I2CIE
I2C Error IRQ						V	V	V	I2CEIE
UART1/2 TX IRQ			V	V	V	V	V	V	UTXIE
UART1/2 RX IRQ	V	V	V	V	V	V	V	V	URXIE
SPI TX IRQ			V	V	V	V	V	V	STXIE
SPI RX IRQ	V	V	V	V	V	V	V	V	SRXIE
RTC IRQ			V	V	V	V	V	V	RTCIE
WDog IRQ			V	V	V	V	V	V	WDTIE
TMA IRQ			V	V	V	V	V	V	TMAIE
TMB IRQ			V	V	V	V	V	V	TMBIE
TMC IRQ			V	V	V	V	V	V	TMCIE
ADC IRQ			V	V	V	V	V	V	ADCIE
CMP IRQ	V	V	V	V	V	V	V	V	CPIE
OPAMP IRQ					V	V	V	V	OPOIE
PT1 IRQ	V	V	V	V	V	V	V	V	PT1IE
PT2 IRQ	V	V	V	V	V	V	V	V	PT2IE
Debug Exception						V	V	V	EDM

31.3. Register function

SoC Status Base Address + 0x04 (0x40104)									
Symbol	SoC Status Register								
Bit	[31:24]					[23:16]			
Name	ICE Configuration					SoC Configuration			
RW	R-0Fh					R-C0h			
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	Reg	F_{PRG}	F_{CRst}	IDLE	$F_{SLP/IDLE}$	F_{WDog}	F_{RST}	F_{BOR}
RW	R0W-0	RW-0	RW0-0		RW-0	RW0-0			RW0-1

Bit	Name	Description	
Bit[06]	F_{PRG}	Power Good flag	
		0	Normal
		1	The Power Good was trigged before.
Bit[05]	F_{CRST}	CPU Core reset flag	
		0	Normal
		1	The ICP Core was trigged before.
Bit[04]	IDLE	Idle mode control bit	

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		0	Sleep mode
		1	Idle mode
Bit[03]	$F_{SLP/IDLE}$	Sleep/Idle Flag(low voltage reset or reset circuit reset can clear the bit.)	
		0	Normal
		1	The chip enters the sleep mode or idle mode.
Bit[02]	F_{WDT}	WDT flag (the low voltage reset or external reset can clear the bit.)	
		0	Normal
		1	The reset or interrupt is generated by the WDT.
Bit[01]	F_{RST}	External reset flag (the low voltage reset (BOR) can clear the bit.)	
		0	Normal
		1	The RESET PIN reset or ICP software reset has occurred.
Bit[00]	F_{BOR}	Low voltage reset (BOR) flag (it will be automatically cleared when the voltage of the chip is high than 1.8V.)	
		0	Normal
		1	The low voltage reset has occurred.

Mode	Setting	Description
Wait Mode	sys_04=0xFF10; asm("syscall 13");	//Idle Set //Wait Mode
Idle Mode	sys_04=0xFF10; asm("syscall 11");	//Idle Set //Idle Mode
Sleep Mode	sys_04=0xFF00; asm("syscall 12");	//Sleep Set //Sleep Mode

SYS_04 Address = 0x40104

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32. LCD DRIVER

32.1. Overall description

The LCD driver circuit is for the TN-LCD and SYN-LCD, and it has the following features:

Built-in voltage regulating circuit (Regulated charge pump)
4-stage adjustable driving voltage levels
Support four kinds of LCD waveform operation
- 1/3 Duty, 1/3 bias. (3-mux,1/3bias)
- 1/4 Duty, 1/3 bias. (4-mux,1/3bias)
- 1/5 Duty, 1/3 bias. (5-mux,1/3bias)
- 1/6 Duty, 1/3 bias. (6-mux,1/3bias)

Selectable input clock sources and programmable output frequency
Blinking capability

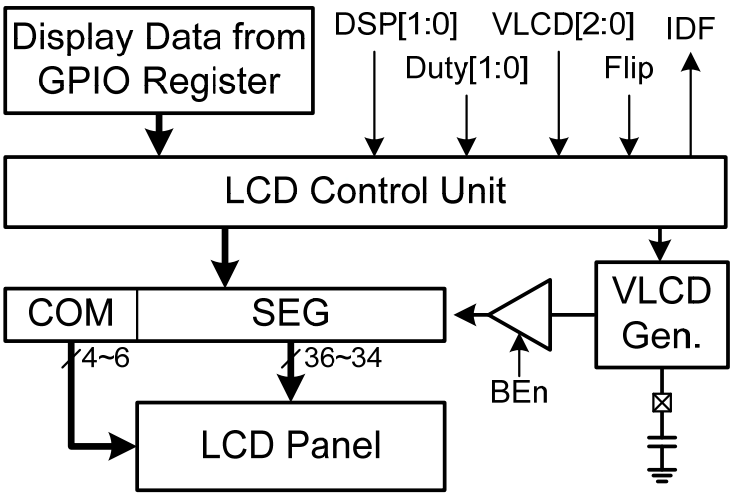

FIG. 32-1 LCD structure diagram

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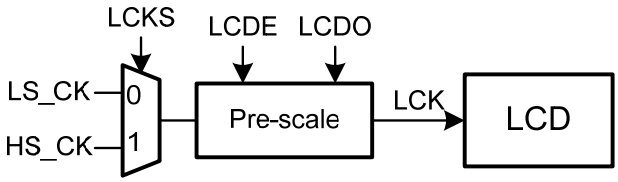
32.2. LCD initialization configuration

Operating frequency and output frame frequency configurations.

The operating frequency can be provided by the LS_CK or HS_CK, which will pass two frequency dividers, LCDE and LCDO to provide proper operating frequencies for the LCD output frame frequency. The LCD operating waveform can be set by the output waveform controller Duty[1:0]; the frame frequency and the operating waveform should be set according to the specification of the LCD to be connected, or ghost shadow, work section or other abnormal phenomena may take place on the LCD. The operating of the LCD is as shown in the following table.



Voltage-doubling circuit and LCD operating voltage configuration

The operating voltage source of the LCD is VLCD; there are two methods to generate it: The VLCD voltage source is inputted from outside, and it is necessary to set the VLCD[2:0] as <0> and disable the voltage-doubling circuit; then, the voltage should be inputted from the external VLCD pin to determine the LCD operating voltage. When driving the LCD of big size or load, the LCD output buffer Ben[0] should be set as <1> to enable the buffer in order to increase the driving ability of the LCD. On the contrary, if the Ben[0] is set as <0>, the buffer will be disabled to decrease the current consumption of the LCD..

The different LCD voltage sources can be generated from the internal voltage-doubling circuit by setting the voltage-doubling circuit controller VLCD [2:0] as <2~5> to make it not vary with the operating voltage of the chip to influence the operation of the LCD. The VLCD [2:0] cab be set to provide four different operating voltages, but the voltage-doubling circuit should be enabled; besides, the voltage-doubling circuit may influence high resolution conversion performance of the A/D converter SD18. When the internal voltage-doubling circuit is used to generate the VLCD voltage source, the Ben[0] buffer will be automatically enabled by the internal hardware circuit.

32.3. Register address

LCD Register Address	31 24	23 16	15 8	7 0
LCD Base Address + 0x00 (0x41B00)	Mask0	REG0	Mask1	REG1
LCD Base Address + 0x04 (0x41B04)	PT9LEn	PT8LEn	PT7LEn	PT6LEn
LCD Base Address + 0x08 (0x41B08)	-	-	-	REG2

-Reserved

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32.4. Register function

32.4.1. Register LCDCR0

LCD Base Address + 0x00 (0x41B00)						
Symbol	LCDCR0 (LCD Control Register 0)					
Bit	[31:24]	[23:21]	[20]	[19:18]	[17:16]	
Name	MASK	-	IDF	-	DSP	
RW	R0W-0	-	R-1	-	RW-0	
Bit	[15:8]	[7]	[6]	[5:4]	[3]	[2:0]
Name	MASK	-	Flip	Duty	BEn	VLCD
RW	R0W-0	-	RW-0	RW-1		RW-0

Bit	Name	Description	
Bit[20]	IDF	LCD Idle control flag	
		0	Active
		1	Idle
Bit[17~16]	DSP	LCD display mode	
		00	Normal mode
		01	The LCD is turned on no matter what the input is.
		10	The LCD is turned off no matter what the input is.
		11	Normal mode
Bit[6]	Flip	Reverse the order between COM and SEG.	
		0	Normal
		1	Inversed
Bit[5~4]	Duty	LCD operating period selection	
		00	1/3 Duty
		01	1/4 Duty
		10	1/5 Duty
		11	1/6 Duty
Bit[3]	BEn	VLCD buffer control	
		0	Disable
		1	Enable(it should be enabled and the functions of the LCD can be used normally.)
Bit[2~0]	VLCD	VLCD mode	
		000	Disable(Charge Pump is disabled, VLCD R is disabled, VLCD buffer is disabled)
		001	R-Type(Charge Pump is disabled, VLCD R is enabled)
		Mode1	Data1=00_011B_3.43V(Charge Pump is enabled, VLCD R is disabled)

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		Mode2	Data1=00_100B_3.16V(Charge Pump is enabled, VLCD R is disabled)
		Mode3	Data1=00_101B_2.93V (Charge Pump is enabled, VLCD R is disabled)
		Mode4	Data1=11_101B_2.73V (Charge Pump is enabled, VLCD R is disabled)
		Mode5	Data1=01_101B_2.55V (Charge Pump is enabled, VLCD R is disabled)
		110	Disable (Charge Pump is disabled , VLCD R is disabled, VLCD buffer is disabled)
		111	Disable (Charge Pump is disabled, VLCD R is disabled , VLCD buffer is disabled)

Data bit1:0X41F24[EN_Rshift1,EN_Rshift0],0X41B00[VLCD2, VLCD1, VLCD0]

32.4.2. LCD register LCDCR1

LCD Base Address + 0x04 (0x41B04)		
Symbol	LCDCR1 (LCD Control Register 1)	
Bit	[31:24]	[23:16]
Name	PT9LEn	PT8LEn
RW	RX-0	
Bit	[15:8]	[7:0]
Name	PT7LEn	PT6LEn
RW	RX-0	

Bit	Name	Description	
Bit[31~24]	PT9LEn	PT9.x mode selection	
		0	I/O mode
		1	LCD mode
Bit[23~16]	PT8LEn	PT8.x mode selection	
		0	I/O mode
		1	LCD mode
Bit[15~8]	PT7LEn	PT7.x mode selection	
		0	I/O mode
		1	LCD mode
Bit[7~0]	PT6LEn	PT6.x mode selection	
		0	I/O mode
		1	LCD mode

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LCD register LCDCR2

LCD Base Address + 0x08 (0x41B08)			
Symbol	LCDCR2 (LCD Control Register 2)		
Bit	[31:16]		
Name	-		
RW	-		
Bit	[15:4]	[3:2]	[1:0]
Name	-	COMLEn	PT10LEn
RW	-	RX-0	RX-0

Bit	Name	Description	
Bit[3~2]	COMLEn	COM5/COM4 mode selection	
		0	I/O mode
		1	LCD mode
Bit[1~0]	PT10LEn	PT10.x mode selection	
		0	I/O mode
		1	LCD mode

LCD register LCDCR3

LCD Mode Base Address + 0X24 (0X41F24)			
Symbol	LCDCR0 (LCD Control Register 0)		
Bit	[31:24]	[23:16]	
名稱	MASK	-	
RW	R0W-0	-	
Bit	[15:8]	[7:2]	[1:0]
名稱	MASK	-	EN_RShift
RW	R0W-0	-	RW-0

位元	名稱	描述	
Bit[1:0]	EN_RShift	EN_RShift	
		1	Set 1
		0	Set 0

Register address 0X41F24 Need to control MASK corresponding BIT1 ~ BIT0

VLCD All Mode View:

Add	0X41F24		0X41B00			MODE
Bit	1	0	2	1	0	
Name	EN_Rshift	EN_Rshift0	VLCD0	EN_Rshift1	EN_Rshift0	V
[01]	0	0	0	1	1	VLCD=3.43V
[02]	0	0	1	0	0	VLCD=3.16V
[03]	0	0	1	0	1	VLCD=2.93V
[04]	1	1	1	0	1	VLCD=2.73V
[05]	0	1	1	0	1	VLCD=2.55V

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33. MODIFICATION RECORD

The following is the important modification of the document, but it does not include the changes of the punctuation and character form.

Date	Document version	Page	Remark
2014/10/01	V01	All	First Edition.

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